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THE TIMING SYSTEM FOR PETRA IV

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Abstract

At DESY, the PETRA III synchrotron light source upgrade towards a fourth-generation, low-emittance machine PETRA IV is being pursued. The realisation of the new machine requires a complete redesign of the timing system, as the beam quality and beam control requirements will change significantly. The new timing system must generate and distribute facility-wide precise clocks, trigger signals, trigger events and beam-synchronous information. The design of the main hardware components will be based on the MTCA.4 standard, which has become a well-established platform at DESY and has successfully been in use with DESY FEL's MTCA.4-based timing systems for almost a decade now. This paper presents and discusses the PETRA IV timing system's overall concept and functionality and its hardware components' development status.

INTRODUCTION

The PETRA IV project [1] involves the replacement of the existing 3rd generation synchrotron radiation source PETRA III with a state-of-the-art ultra-low emittance storage ring. That includes the upgrade of the storage ring infrastructure with a circumference of 2304 m, as well as the redesign of the current pre-accelerator chain and the construction of new beamlines. The 6 GeV storage ring will be operated at an RF frequency of 500 MHz as PETRA III.

The present booster synchrotron DESY II will be replaced by a new one, DESY IV, to meet the requirements of a low emittance beam injected into PETRA IV. While the LINAC II section will be kept, the gun will be upgraded, and the transfer section with the PIA accumulator will be revised. As an alternative to the DESY IV and LINAC II injector chain, developing and constructing a plasma-based injector will also be part of the PETRA IV project.

The front-end electronics for diagnostics and instrumentation for the PETRA IV accelerator will be entirely overhauled and based on the MTCA.4 standard. At the same time, the existing PETRA III control system will be changed over to a DOOCS-based one as used at the DESY FEL accelerators. That effectively leads to the necessity to redesign the entire timing and synchronization system and its controls for the storage ring as well as for the pre-accelerator chain.

RF SYNCHRONISATION

The essential requirement of the RF synchronisation system is to provide a continuous reference RF signal generated by a unique, stable master oscillator to drive local, low-noise oscillators. The fundamental RF frequency for the PETRA IV storage ring has to be 499.6643 MHz, while the 3rd harmonic RF system requires a reference RF frequency of 1.4989929 GHz. The DESY IV booster will have the same frequency as PETRA IV, while the PIA accumulator will be operated at 125 MHz, which will be derived from the DESY IV RF reference. The plasma-based injector will have a laser system operated at 2.9979858 GHz, but the injector itself will work at the same frequency as PETRA IV.

The RF synchronisation system will consist of three RF synthesisers in total. One for PETRA IV, one for the booster chain and one for the plasma-based injector. Redundant GPS Rubidium standards will provide a 10 MHz reference to these synthesisers. Each Rubidium standard has a GPS antenna for high reliability and is compensated for environmental impacts and component ageing. In normal operation, the synthesisers are coupled and generate a phase-synchronous frequency of 499.6643 MHz.

The PETRA IV system will supply, in addition, a 1.4989929 GHz reference for the 3rd harmonic system, while the plasma-based injector system will provide an additional 2.9979858 GHz signal for the laser system. The 499.6643 MHz will be adjustable in the range of +/-1.5 kHz, and the 3rd harmonic frequency in the range of +/-4.5 kHz. This feature will be used for non-standard operations like the aforementioned dispersion measurement. It requires decoupling the RF synthesisers while the frequency is being swept over this range.

When going back to normal operations, the frequency of the DESY IV system, resp. of the plasma-based injector system, needs to be driven in a phase-continuous way until the PETRA IV frequency is matched again. For this, the synthesiser has to be capable of Direct Digital Synthesis (DDS).

The RF references from each synthesiser provide a direct, high-quality, high-power RF reference signal to the RF systems and the central timing system components for PETRA IV and the injector chains. A direct distribution of the high-quality, low-noise and high-power RF reference signal is foreseen not only for the RF systems but also for dedicated customers, e.g. the multi-bunch feedback system and beamline experiments. This is done by using standard RF cables placed into the PETRA IV tunnel to profit from the temperature-stabilised environment.

The RF cables must be chosen to keep at the minimum the losses along the path in the tunnel. Distribution racks in the experimental supply halls, the DESY IV, PIA and LINAC II supply halls are currently planned, each having a redundant, direct connection to the central system. The distribution racks will be equipped with amplifiers and splitters for further distribution to customers, like beamline hutches and experiments. At those locations where both RF-synchronisation and fibre optical distribution are present, one system can act as a backup of the other one.

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TIMING SYSTEM

The timing system will provide a continuous timing signal for synchronisation purposes, i.e., a bunch trigger based on the revolution frequency of 130.1 kHz marking the first bunch position in time in the PETRA IV storage ring. The system will generate and distribute various configurable event-based trigger signals according to the beam mode (e.g. beam injection and extraction trigger) and provide low-jitter machine clocks (e.g., 500 MHz, 125 MHz or 10 MHz) for measurement equipment and experiments. It will distribute a postmortem trigger and supply beam status information (e.g. beam dump or top-up mode), the fill pattern and the actual bunch pattern, beam currents and a unique beam revolution number. All the timing information will be distributed from a central source to local clients via a redundant optical fibre network, as shown in Fig. 1. The fibre connections will be path-length compensated for local environmental impacts.

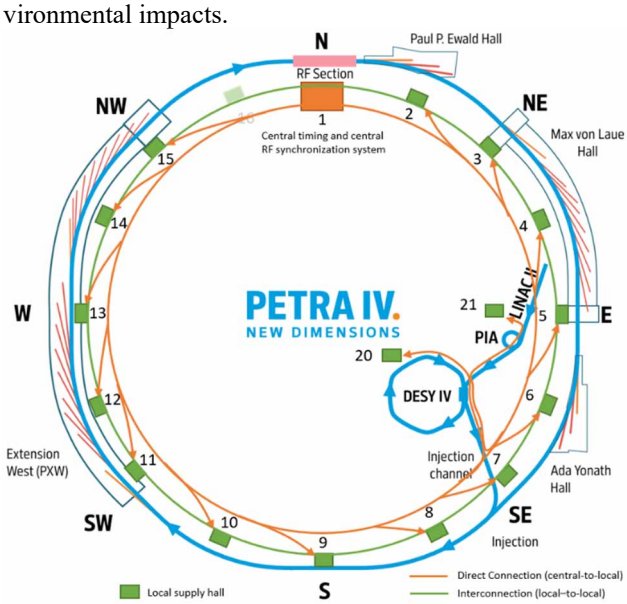

Figure 1: Topology of the optical fibre distribution for the timing system.

Each of the central timing systems will comprise a 9U 12-slot MTCA.4 (Micro Telecommunications Computing Architecture) [2] crate system, equipped with two redundant 1 kW power supplies, two cooling units, one host MTCA.4 CPU AMC (Advanced Mezzanine Card), one MCH (Management Controller Hub) and several DAMC-X3TIMER modules, which are the main hardware components of the timing system. The DAMC-X3TIMER AMC will be configured to operate either as a transmitter, when used as a central module, or as a repeater or receiver. In addition, Rear Transition Modules (RTM) will be developed and mounted on the back of the DAMC-X3TIMER slots to distribute clock and trigger signals to various PETRA IV systems. At maximum, a 12-slot crate can be equipped with ten timing modules. However, one of those slots will be reserved for the interface to the Machine Protection System.

The first timing module in the main timing crate serves as the heart of the overall timing system. All the other timing modules function as repeaters, redistributing the timing system's signals and information. The optical fibre cables will primarily be routed through the PETRA tunnel sections in the experimental halls alongside the tunnel on dedicated cable trays, using a tube system for easy deployment and potential later enhancement or replacement of individual fibre bundles. The fibres will be single-mode fibres with a 9/125 µm diameter suitable for wavelengths ranging from 1270 nm to 1550 nm and equipped with LC/PC connectors on both ends. For the best performance of the active drift compensation, bi-directional optical Small Form-factor Pluggable (SFP) transceivers with wavelength multiplexed transmission and reception on the same fibre will be used. Each local supply hall will host a temperature-controlled rack holding an MTCA.4 crate for redistributing the timing information.

The crate will house two redundant 1 kW power supplies, two cooling units, one MCH, and one host CPU AMC. All ten slots will be equipped with DAMC-X3TIMER modules and RTMs. Each AMC-RTM pair could serve 12 individual connections for redistribution, allowing 120 connections per crate in its default configuration. If required, up to two additional MTCA.4 crates can be installed in the existing rack. Local clients of the various accelerator subsystems and beamline experiments will be connected to the redistribution crates by optical patch cables. Accelerator subsystems will place their electronics in the same supply halls.

In general, those are mostly MTCA.4 based systems. Hence, a DAMC-X3TIMER plugged into those systems will function as the end receiver and local timing system client. The local client DAMC-X3TIMER AMC will be part of the corresponding subsystem. Beamline experiments will have a connection routed to their hutches, where the MTCA.4 crates with a DAMC-X3TIMER AMC will be located. The fibre cable topology will allow receivers with high requirements for the input signals to be connected directly to the transmitter; all others can use the redistribution crates. A schematic overview of the MTCA arrangement is shown in Fig. 2.

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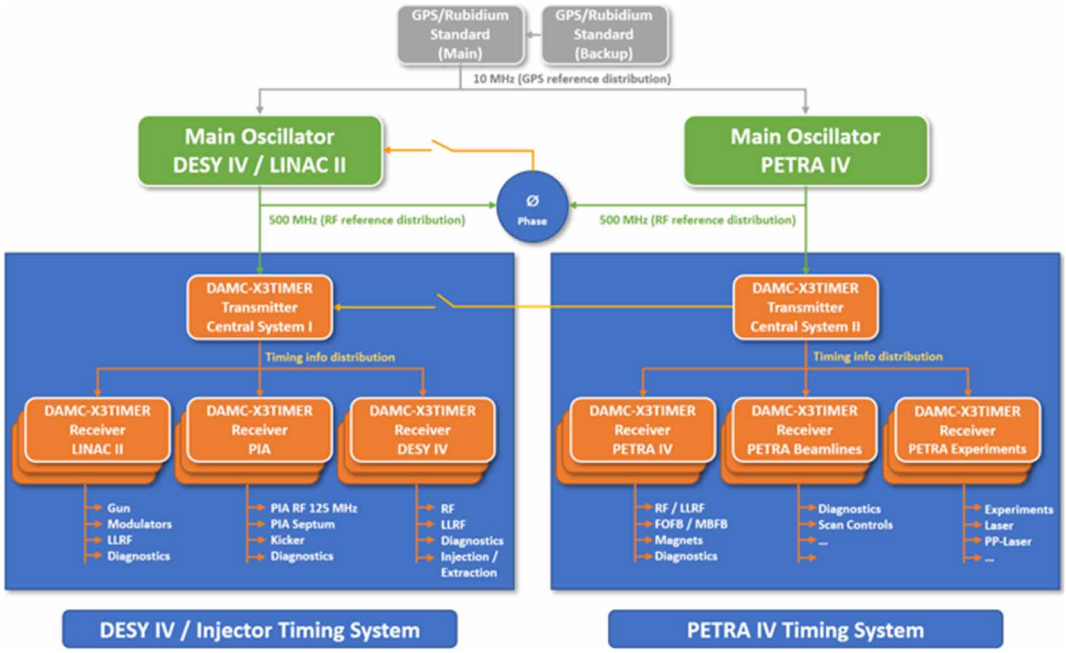

Figure 2: Schematic view of the timing systems topology representing the configuration of PETRA IV and the booster DESY IV as an injector chain.

Implementation

The hardware and the control software for the timing and RF synchronisation systems of PETRA IV and the injector systems will have to be built brand new. Many components operated at PETRA III have already been used in previous generations of the storage ring, and their service life has practically elapsed. The implementation of the new PETRA IV system will be based on the MTCA.4 electronics standard, the upcoming de facto standard within the accelerator community. Apart from that, the successful deployment and operation of the MTCA.4-based timing system at the European XFEL and the FLASH facility using the X2TIMER AMC [3], and the profound in-house knowledge and the slight advantages over the commercially available MRF system gave reason to develop a successor model, the DAMC-X3TIMER AMC, based on the X2TIMER concepts and functionality. As mentioned before, the DAMC-X3TIMER AMC can be operated either as a transmitter, using an external RF reference or an internal oscillator for standalone mode, as a repeater for further distribution or as a receiver for local timing system clients. The DAMC-X3TIMER transmitter will generate a timing data stream consisting of clock and trigger signals and beam-synchronous data and broadcast the data stream over the optical fibre. The rate at which the data is transmitted will be driven by the reference frequency received from the RF synthesiser. The DAMC-X3TIMER receiver will recover the RF frequency from the data stream using the clock data recovery (CDR) technique. The recovered clock will be fed to an on-board dual loop clock cleaner, which contains two Phase-Locked Loops (PLLs) to reduce the clock jitter. Since PETRA IV will be operated with an RF frequency of 499.6643 MHz adjustable by +/- 1.5 kHz for thermal adjustment and chromaticity measurements, a customised voltage-controllable crystal oscillator (VCXO) will be used on the DAMC-X3TIMER AMC to ensure that the PLLs provide a sufficient tuning range. The jitter-cleaned clock will be used to derive further clock signals, which will be distributed to the on-board programmable logic device or external components via the front panel, MTCA backplane and RTM modules. The DAMC-X3TIMER AMC transmitters and repeaters will also provide drift compensation to keep the propagation delay to the corresponding receivers constant over temperature and humidity changes. For this, each receiver will loop back the data stream to the transmitting/repeating module. A dedicated hardware unit on the transmitting/repeating AMC will detect the phase difference between the local system clock and the recovered clock from the received data stream. A control loop will configure dedicated delay lines in the Rx and Tx paths to keep the phase relation constant. The measured phase difference and the delay values can be read out and provided to the control system for diagnostics. Since not every AMC needs drift compensation, this function will be implemented on a daughter module that can be mounted optionally on the DAMC-X3TIMER main board. Each DAMC-X3TIMER AMC will use a programmable logic device, either a Field-Programmable Gate Array (FPGA) or a System-on-a-Chip (SoC) FPGA, for real-time clock-synchronous signal and data reception, processing and distribution. A PCIe interface to the host CPU AMC via the MTCA backplane will allow for device configuration, software interrupt and data transmission, configuration and monitoring of on-board peripherals and firmware updates. The functionality of the programmable logic device is described in the firmware section. A set of Rear Transmission Modules (RTM) will be developed to extend the DAMC-X3TIMER for custom use cases. The pinning of the Zone3 Connector shall follow the DESY

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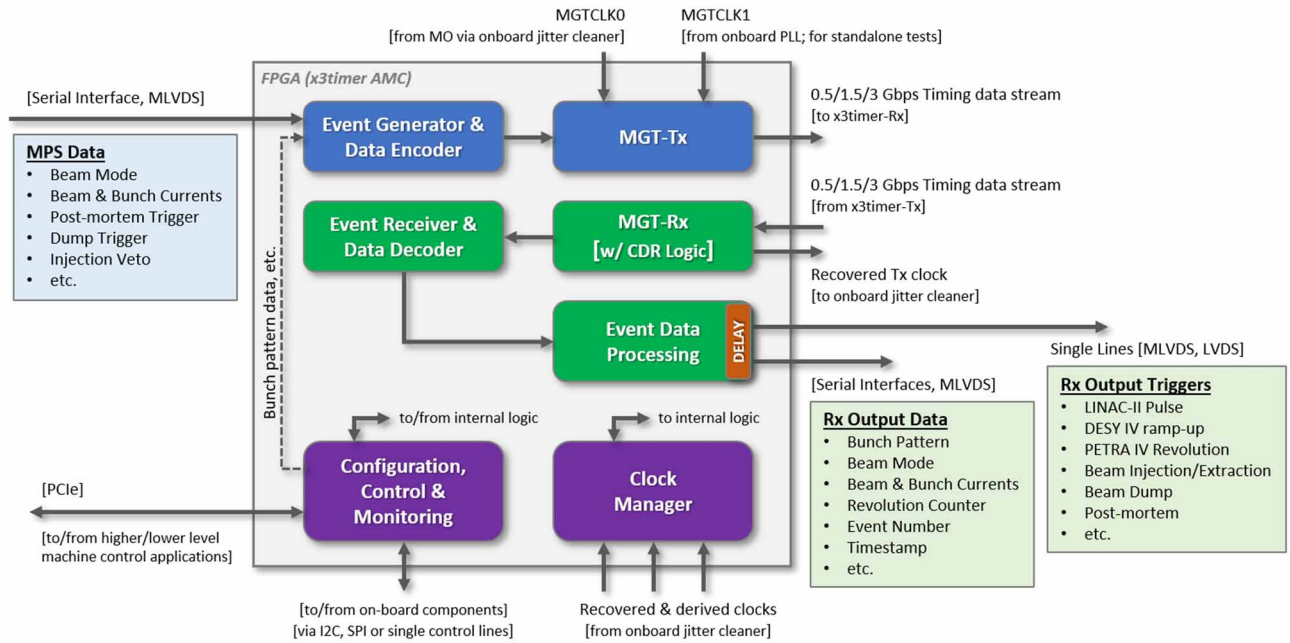

Figure 3: Block diagram of the main functional processes assigned to the programmable logic device on the DAMC-X3TIMER board

recommendation and be designed as Class D1.1, which covers 2 Multi-Gigabit (MGT) lanes and 42 LVDS I/O lines. Foreseen RTM variants cover the extension with outputs for LVDS and TTL level (e.g., also NIM and optical) and with on-board signal fine delay adjustment. Also, a fanout RTM for the timing data stream will be developed. Further, an RTM for high-precision clock output and connection to the RF-Backplane (in MTCA.4.1 standard) is planned.

Firmware

The tasks of generating and distributing timing and beam synchronous signals and data to the PETRA IV subsystems will be assigned to a programmable logic device located on the DAMC-X3TIMER module. The device will be reconfigurable and feature sufficient internal resources to cover the needs of implementing the currently foreseen complex real-time processing and subsequent upgrades determined by possible enhancements in the requirements for the timing system. Fig. 3 illustrates schematically the functionality foreseen to be implemented in the programmable logic device. As with the host AMC, the device will incorporate logic to support both the transmitter and the receiver functionalities. On the transmitting side, the device will have to assemble a timing event block and send it serially to the timing receivers via an internal Multi-Gigabit Transmitter (MGT-Tx), the high-speed electrical links and the optical SFP modules located on the AMC, and optical fibre cables. The timing event block will include:

- Trigger information (e.g., dump trigger, post-mortem trigger, injection veto) and machine configuration and status (e.g., beam mode, bunch pattern table, beam current) received from the MPS via a fast serial interface and from the machine control system via the local CPU and a PCIe interface;
- Locally generated trigger signals (e.g., triggers for the pre-accelerator chain, PETRA IV injection/extraction and revolution triggers);
- Locally generated timing data (e.g., revolution counter, bunch number, event timestamp).

The event data transmission will be driven by a low-jitter clock, derived on the AMC from the RF input received from the RF synthesiser, and will use the 8b/10b encoding to ensure a proper DC balance over long distances and sufficient signal-level transitions for a suitable clock and data recovery on the receiving end. In addition, alignment characters will be inserted in the event data stream to ensure deterministic timing behaviour across the distributed system. For stand-alone tests and verifications in the laboratory environment, the transmission clock will be supplied from an on-board programmable PLL. The transmission rate will depend on aspects like the amount of data that has to be transferred and the update rate requested by the PETRA IV subsystems. The current design considers a baseline rate of 0.5 Gbps, but provisions have already been made to increase it to 3 Gbps if necessary. On the reception of the input stream, the receiver logic will recover the transmission clock and the event data and feed them to different functional entities.

The recovered clock will be routed to the on-board jitter cleaner to derive the clocks needed to drive the internal logic and the external serial interfaces. The recovered event data will be decoded, and the individual trigger signals and timing data will be extracted and distributed to the PETRA IV subsystems that request them via high-speed LVDS/MLVDS links tracing to the MTCA backplane and AMC's front panel. Additionally, global and fine programmable delays will be applied to all the output serial links to compensate for differences in optical fibre length resulting from the different positions of the receiver modules along

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the pre-accelerator chain and the PETRA IV ring. For configuration, control and monitoring purposes, a PCIe interface will connect the programmable logic device with the local CPU via the MTCA backplane. The programmable logic device will distribute the incoming configuration and control data to all internal and on-board programmable locations. In addition, the device will collect various status and monitoring data from distributed internal and on-board functional units and provide them on the PCIe bus upon request from the supervising software.

For the build of the firmware design, the FPGA Firmware Framework for MTCA modules developed by the DESY MSK group will be employed. The framework automates the FPGA/SoC design flow and verification processes, providing support for various EDA tools and FPGA/SoC generations from different vendors, and it integrates the design flow with the Jenkins automation server for regular verifications of code revisions. In addition, the framework can generate register address space files in different formats and for various applications, e.g., synthesisable VHDL modules for firmware development, C/C++ header files for low-level software applications running on the local CPU, and markup-based text files for technical documentation of the FPGA/SoC design.

Control System Software

The timing and synchronisation software will be based on standards like open source-based software solutions and the Distributed-Object-Oriented Control System (DOOCS) [4] framework. The latter has become the standard platform for accelerator controls at DESY. The software part provides access to the hardware and firmware of the timing and RF synchronisation systems for configuration, maintenance, modifications and monitoring purposes. Furthermore, beam-synchronous information like a high-resolution timestamp, revolution counters and a bunch or fill pattern will be made available to sub-systems.

The main component will be a server application for operating the MTCA.4 AMC and its RTM. This server application will be used for each of the central MTCA timing systems, but will also be available on every local client MTCA timing system. In every crate with timing modules, a DOOCS timing device server running on the crate CPU controls the hardware via a PCIe interface. This server will provide all configuration parameters as properties on the global control system network. This device server communicates via a Linux driver with the AMC module. All timing configurations have to pass this server. After a power failure or any other restart of the system, the DOOCS server will restore all timing parameters to the previous state. It is also responsible for restricting access to timing parameters and their modification. Furthermore, there shall be applications to operate and monitor:

- the GPS reference system;
- the main oscillator systems for PETRA IV, the DESY IV booster and its LINAC II, and for the plasma injector;
- the MTCA management of timing system crates;
- general performance of the timing and synchronisation systems.

This set of software has to be complemented by high-level control applications providing the functionality to operate the overall facility (e.g., setting the fill pattern and beam mode), switching between injection mode and idle for DESY IV. Graphical user interfaces will be implemented using the Java DOOCS Data Display (JDDD) framework. The AMC and RTM hardware will be presented through a dedicated JDDD panel where all parameters of the MTCA application server can be inspected and configured. All other applications will each get a dedicated overview and controls panel.

CONCLUSION

The new timing system for the upcoming PETRA IV facility is currently in the design stage and progressing well. Based on the MTCA.4 standard, the new, updated electronics fits well into the existing landscape of the timing systems at the various accelerators at DESY. Utilising the expertise from these and adapting it to the needs and requirements of the new PETRA IV facility and its injector chains will result in beneficial synergy effects. The newly designed MTCA.4 timing module is supposed to meet not only the PETRA IV-specific requirements but also function as a modernised version of the existing module used at DESY's FELs.

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