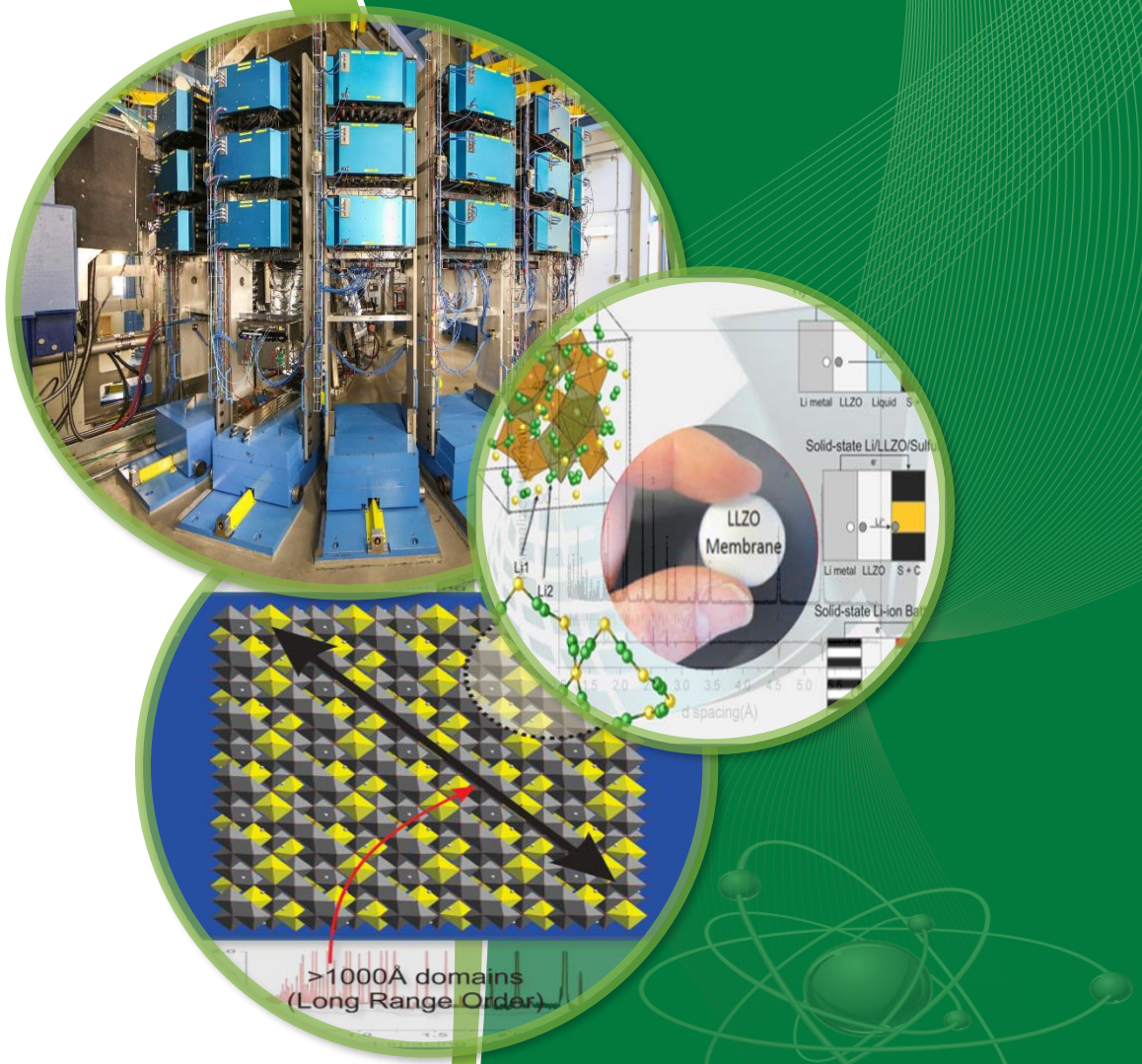
Noise Mitigation For Neutron Detector Data Transport



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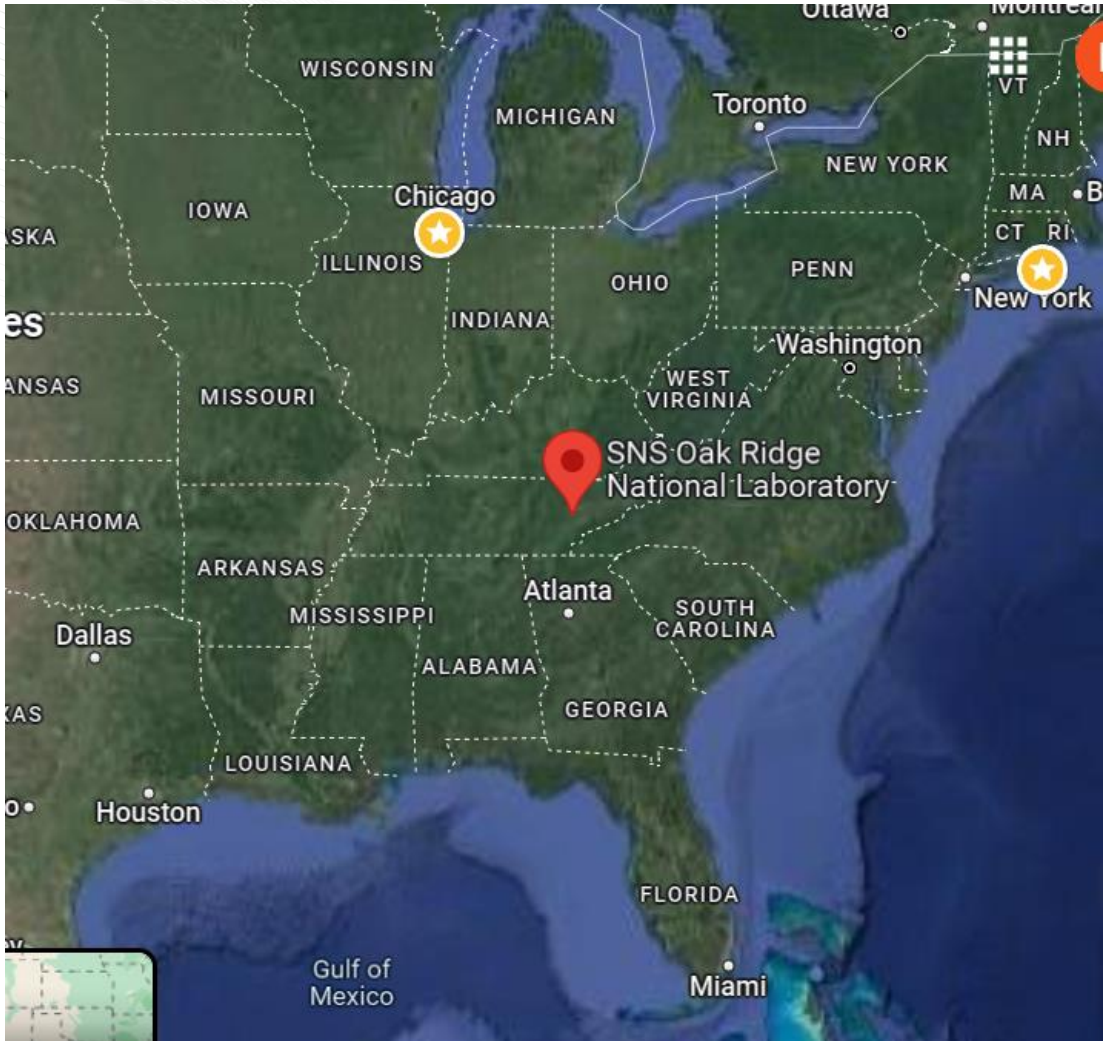
ORNL

ICALEPCS 2023 Cape Town, South Africa
October 9, 2023

WE3AO03

Spallation Neutron Source, High Flux Isotope Reactor



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- SNS
- HFIR
- STS – future neutron source

LVDS data transport; TIA/EIA-644

3.5mA x 100Ω = 350 mV

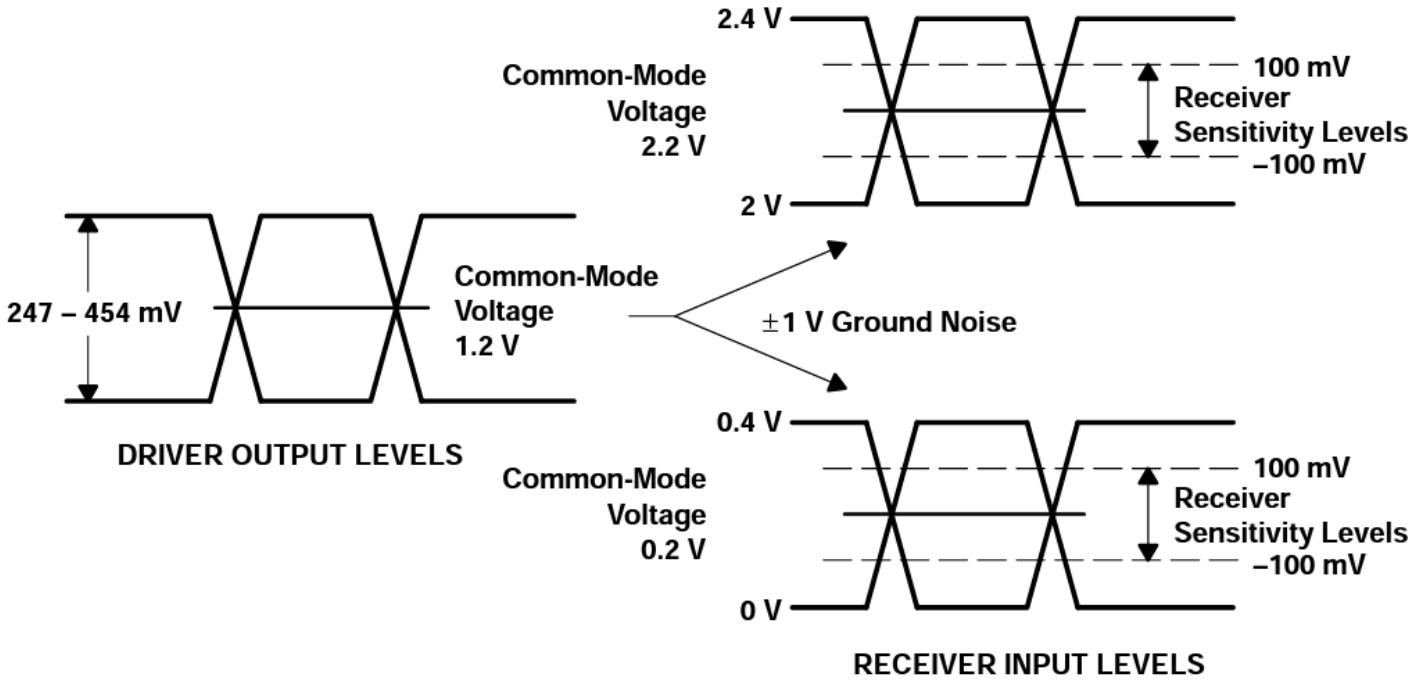
Low-voltage differential signaling (**LVDS**), also known as **TIA/EIA-644**, is a technical standard that specifies electrical characteristics of a differential, serial signaling standard. LVDS operates at low power and can run at very high speeds using inexpensive twisted-pair copper cables. LVDS is a physical layer specification only; many data communication standards and applications use it and add a data link layer as defined in the OSI model on top of it.

The low differential voltage, about **350 mV**, causes LVDS to consume very little power compared to other signaling technologies. At 2.5 V supply voltage the power to drive 3.5 mA becomes 8.75 mW, compared to the 90 mW dissipated by the load resistor for an RS-422 signal.

TIA/EIA-644, otherwise known as LVDS, is a signaling method used for high-speed, low-power transmission of binary data over copper. This signaling technique uses lower output-voltage levels than the 5-V differential standards (such as TIA/EIA-422) to reduce power consumption, increase switching speed, and allow operation with a 3.3-V supply rail. The LVDS current-mode drivers create a differential voltage (**247 mV** to **454 mV**) across a **100-Ω** load. The LVDS receivers detect signals as low as **±100 mV** with as much as **±1-V** *ground noise*.

- LVDS is DC coupled

Ground noise tolerance for LVDS data transport; TIA/EIA-644

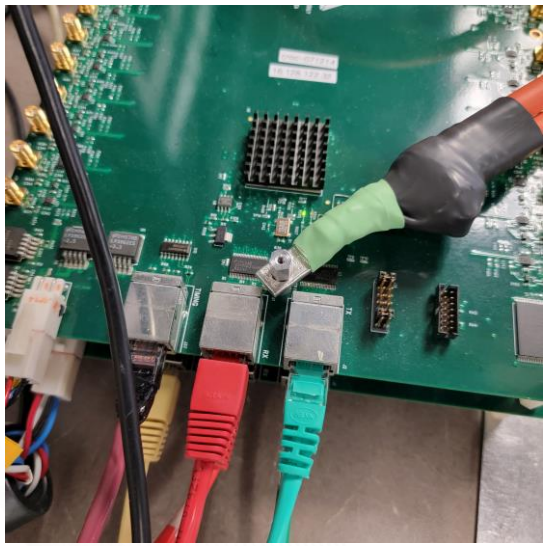


RJ45:

- data 3 pairs (280 MHz); 7 bits each pair
- 40 MHz clock pair 4

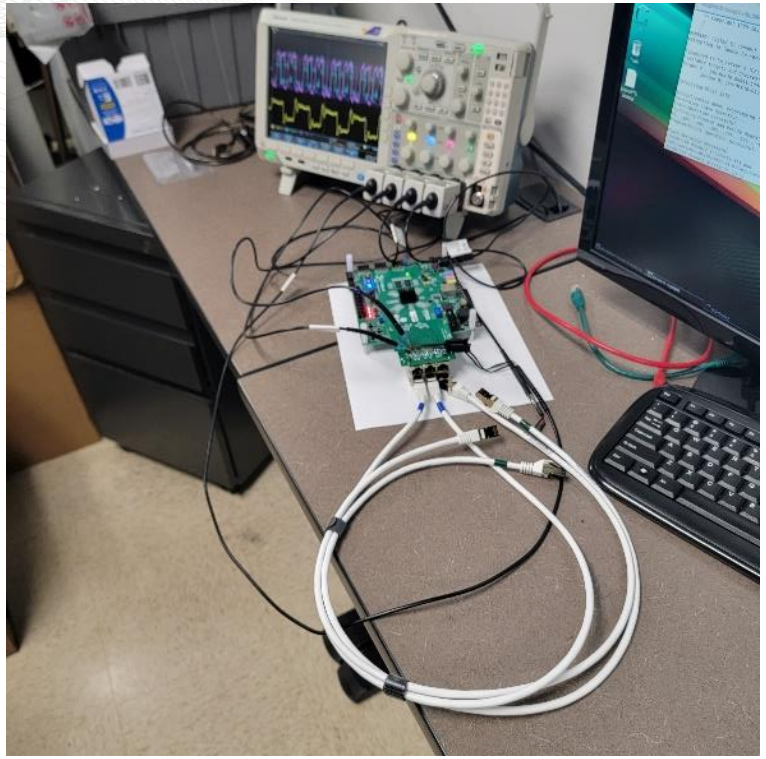
FPGA

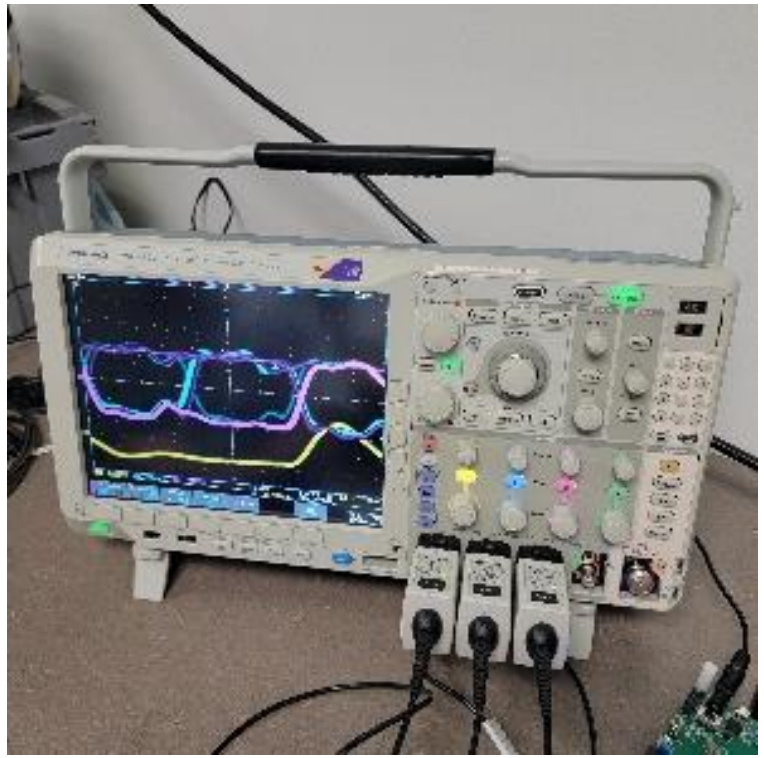
- ROC
- FEM concentrator
- DSP



T/C, Rx, Tx

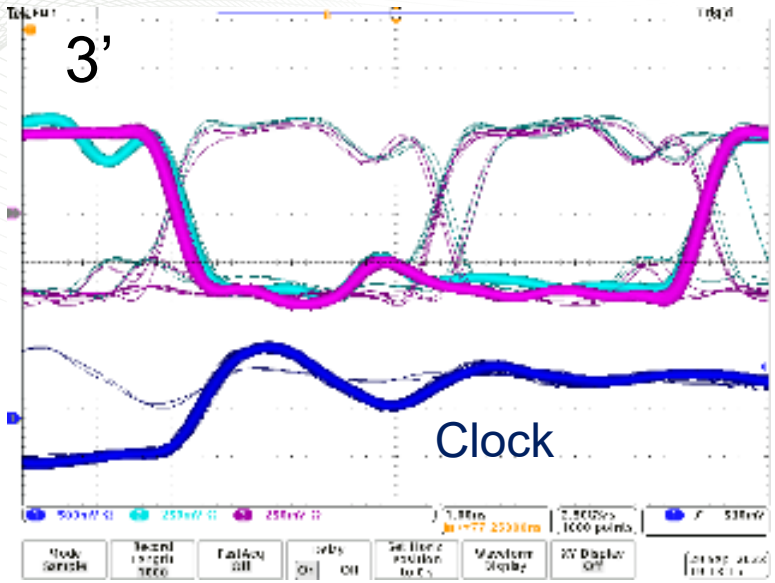
LVDS eye diagram measurement

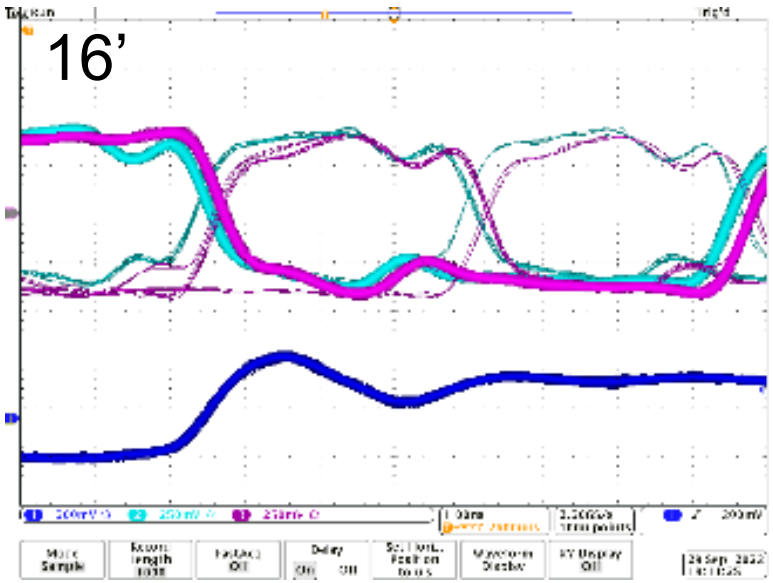


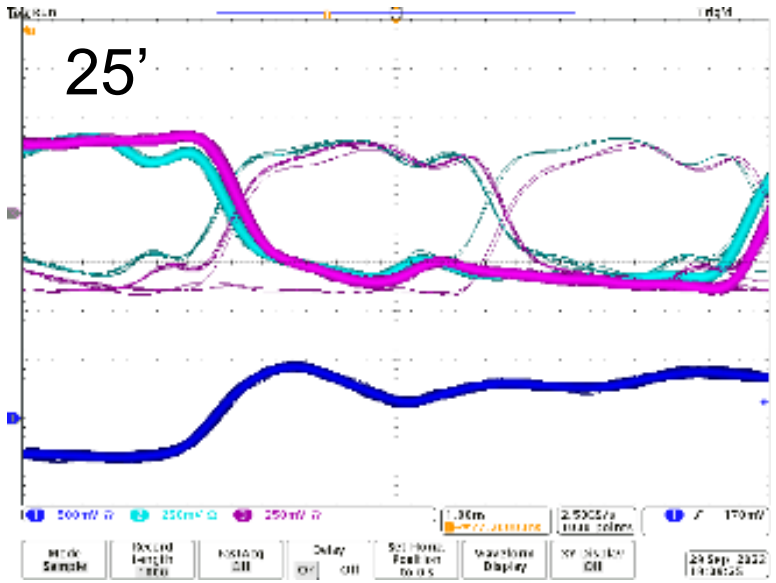


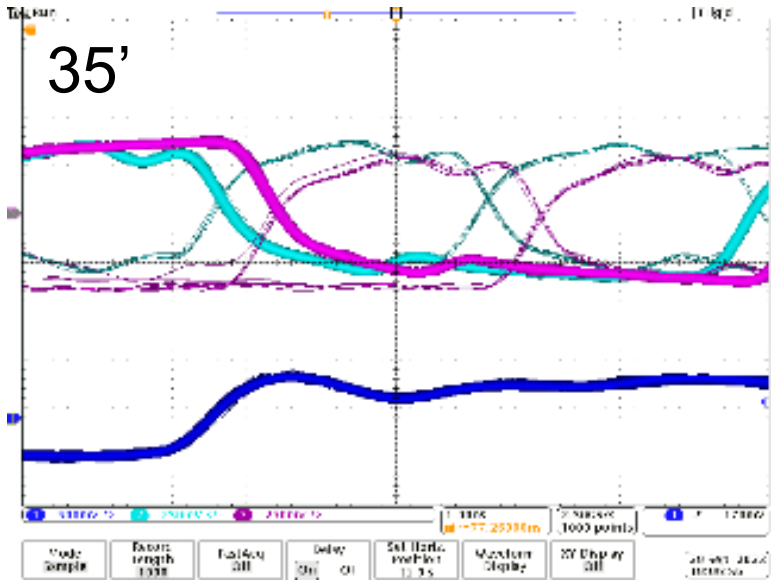
- Tektronix MDO4104B-6 Mixed Domain Oscilloscope, 6 GHz (1 GHz, 5 GS/s)
- LVDS data (280 MHz): Tektronix TDP3500 Differential Probe 3.5 GHz.
- LVDS 40 MHz clock: Tektronix TAP1500 1.5 GHz active probe.

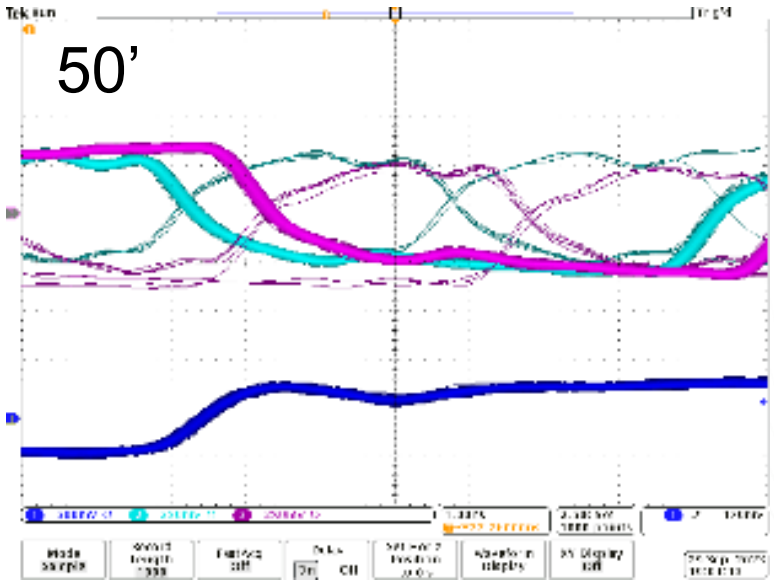
LVDS eye diagram signals: Cat8, RJ45, pin[1,2][4,5]







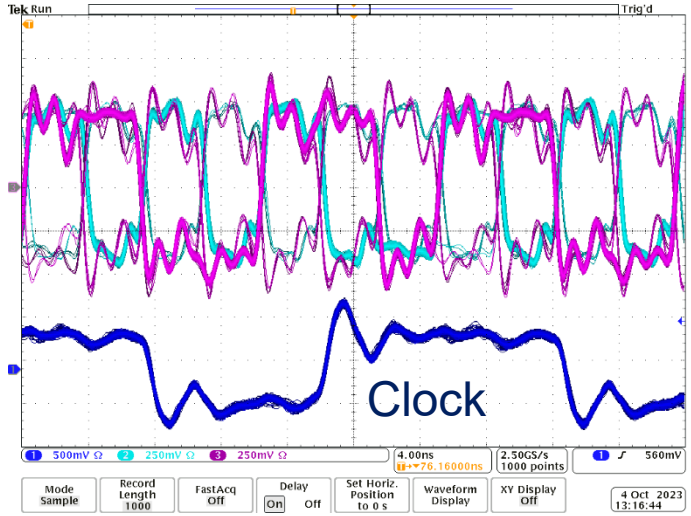




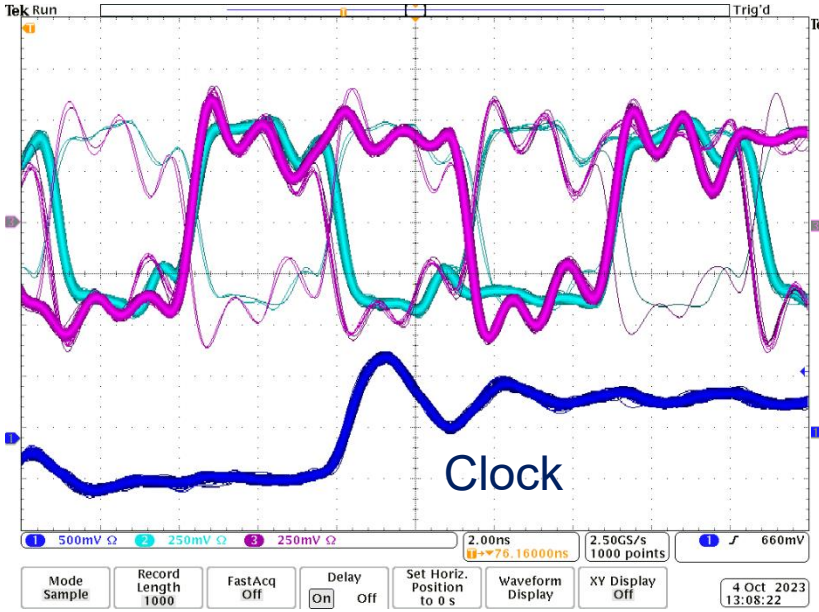
- Skew increases
- Voltage decreases
- Rise time increses

LVDS eye diagram signals

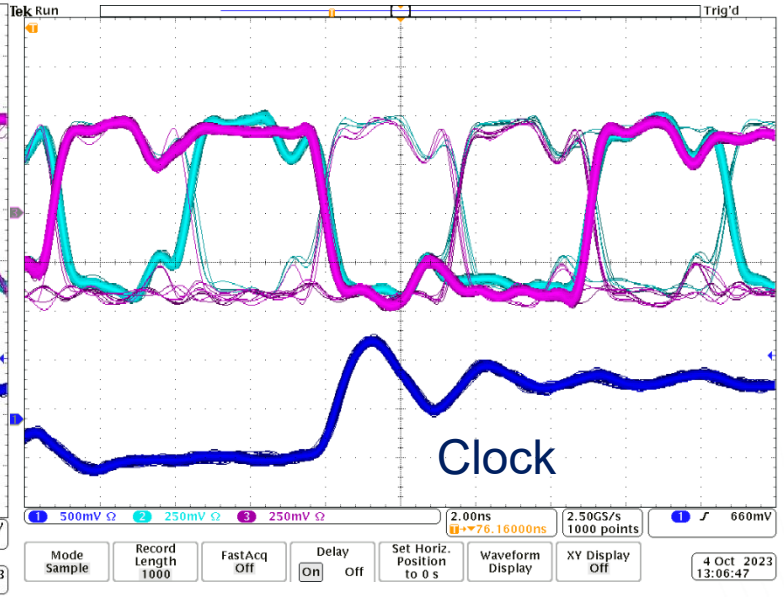
- LVDS, Cat8 cable, 280 MHz data, 40 MHz clock.
- Test hex pattern send: AAAA5555; A=1010101
- R_{AC} (50 feet) ~ 100 Ohm;
  - Skin depth of copper ~ 5um (@280 MHz)
- [R_{DC} (50 feet) = 6.4 Ohm]



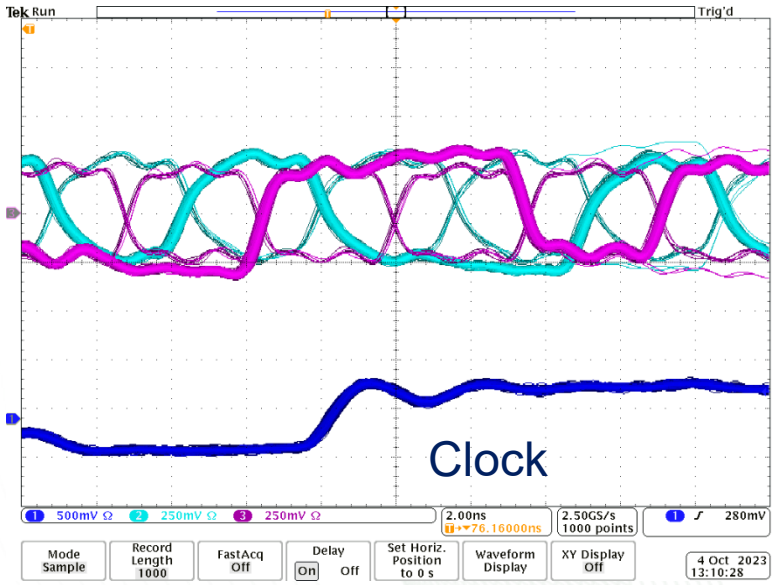
Length=3'; RJ45, pin[1,2][4,5]



Length=3' RJ45, pin[1,2][3,6]



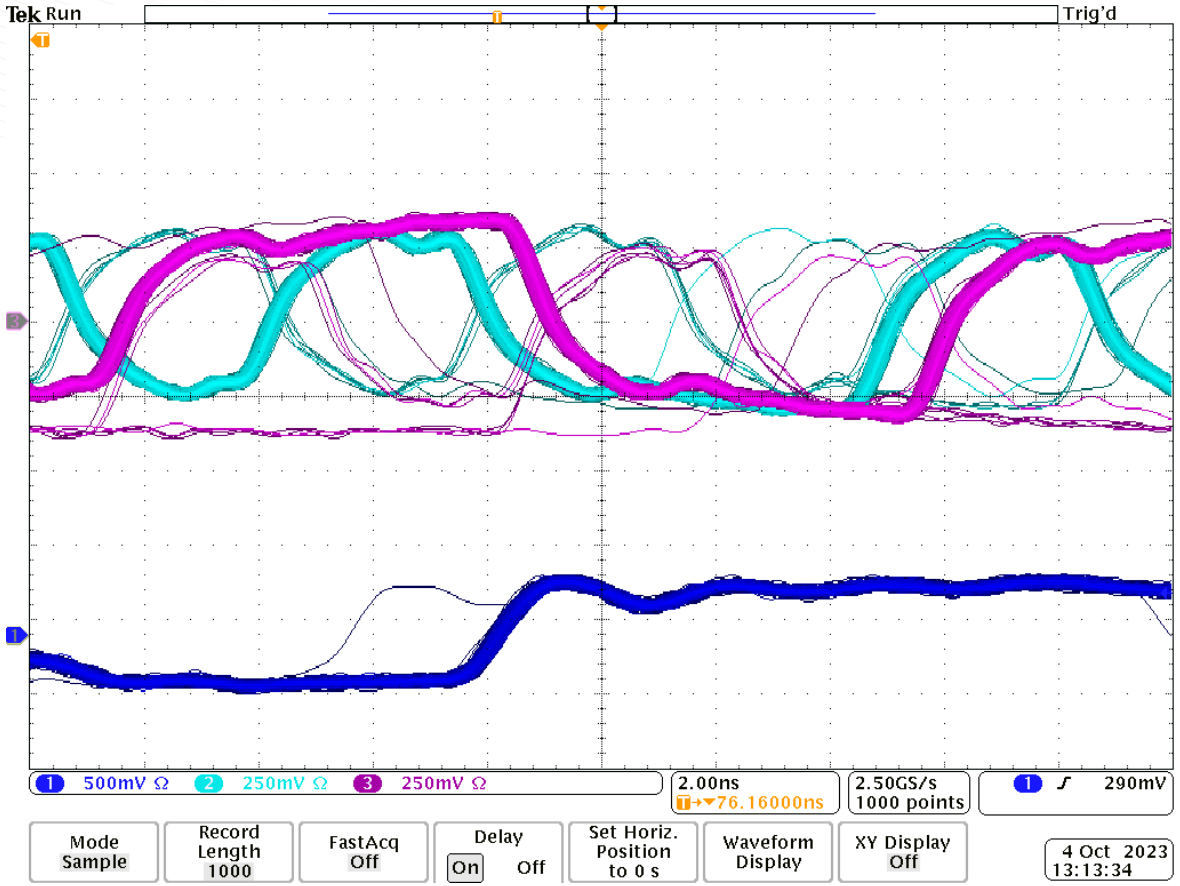
Length=50'; RJ45: pin[1,2][3,6]



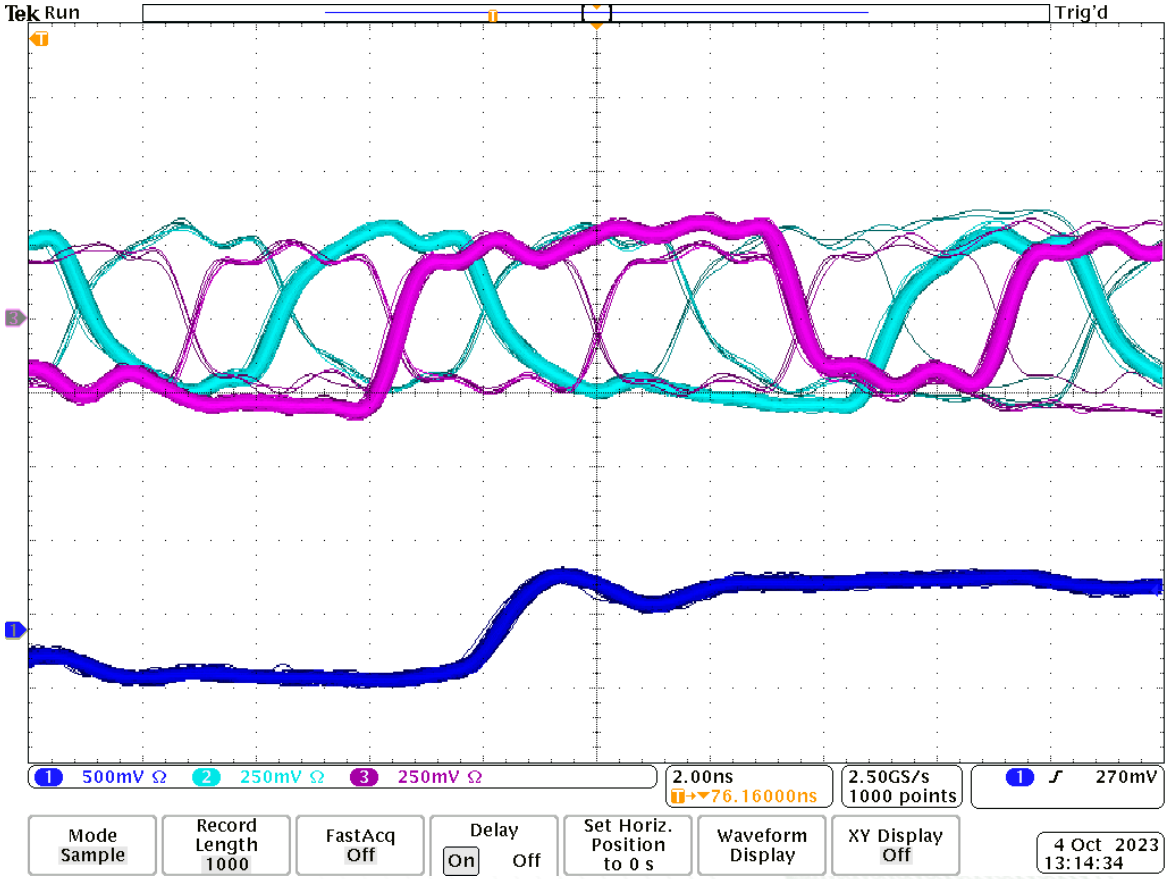
Summary

- LVDS, Cat8 cable

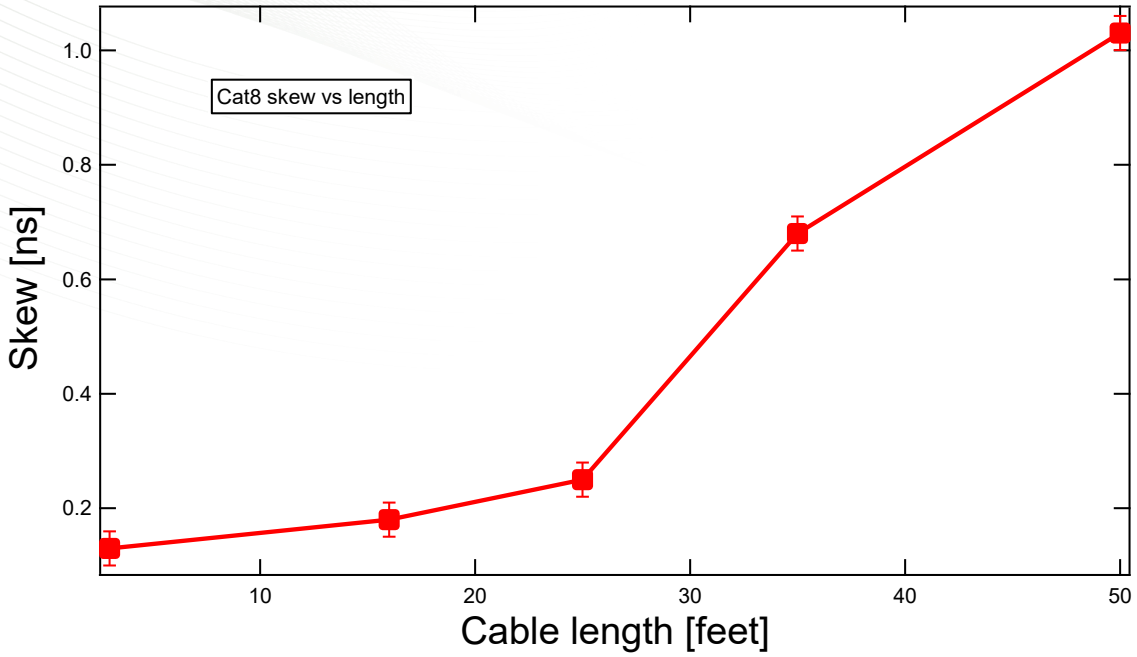
Length=50’; RJ45: pin[1,2][4,5]



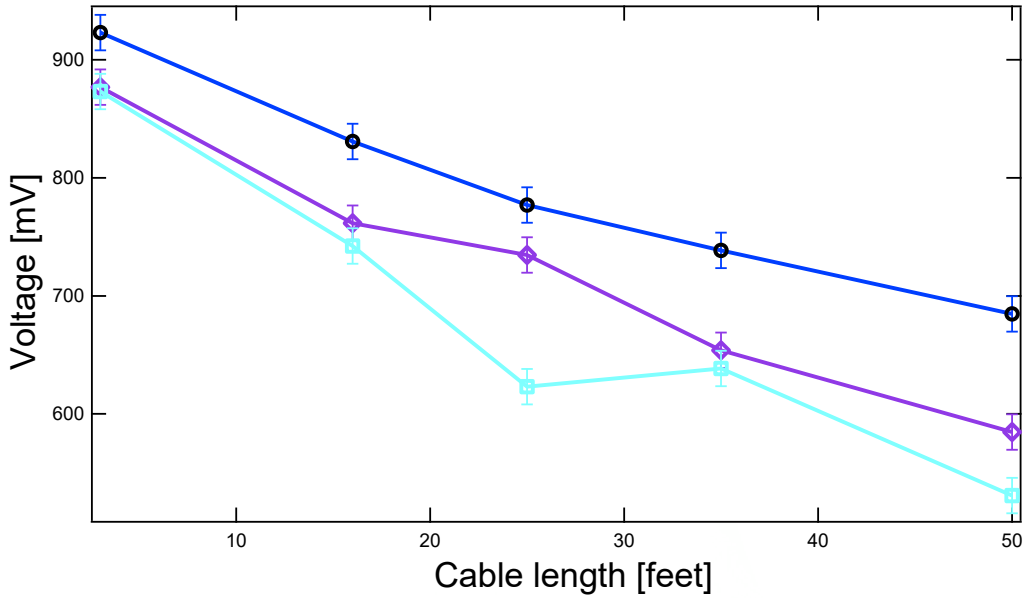
Length=50’; RJ45: pin[1,2][3,6]



LVDS signal skew, signal level vs cable length



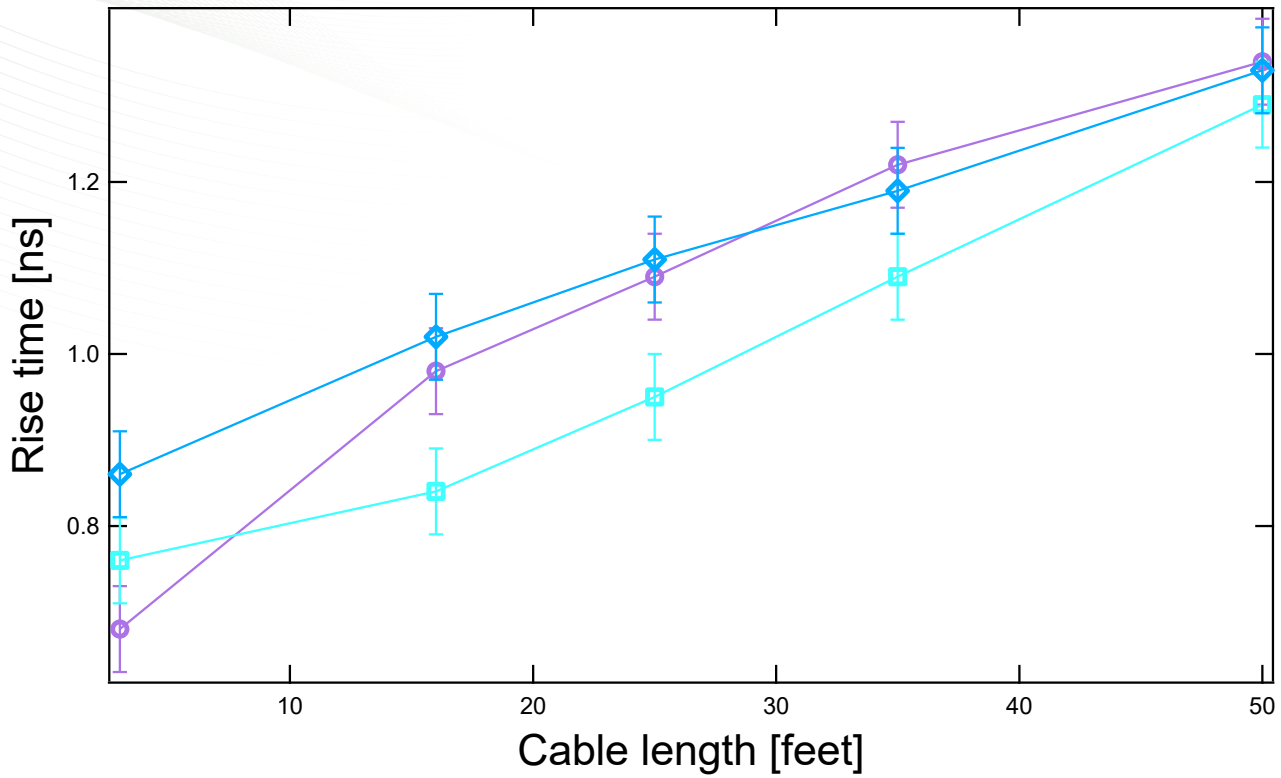
Signal time skew between Cat8 Pair [1,2] and Cat8 Pair [4,5] as a function of cable length.



Signal voltage at receiver as a function of cable length.

Copper skin depth is about 5um, thus 50' cat8 cable resistance is about 100 Ohm. [DC resistance is 6.4 Ohm]

LVDS signal rise time vs cable length.

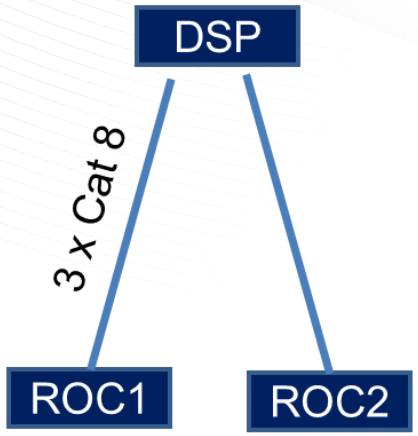


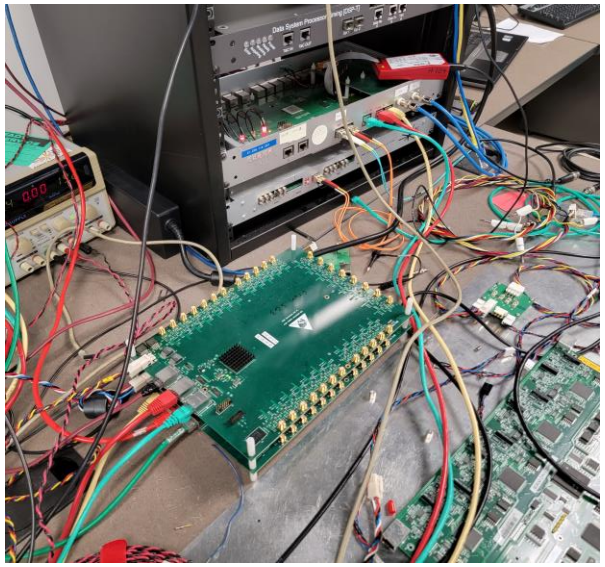
Signal Dispersion in twisted pair cable.
Rise time increases for longer cables.
Impulse response broadened.

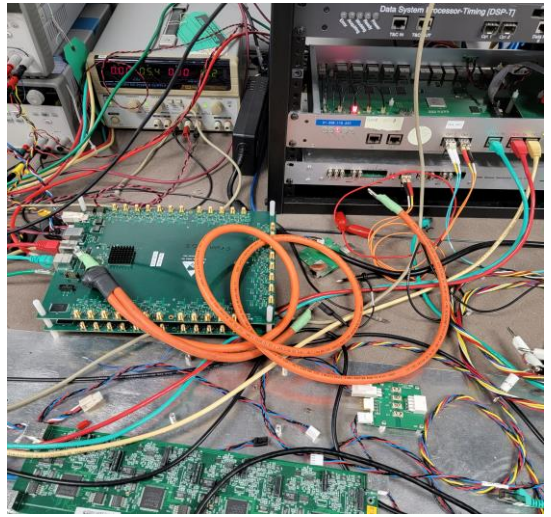
Rise time as a function of cable length.
Features are “washed out” due to dispersion.

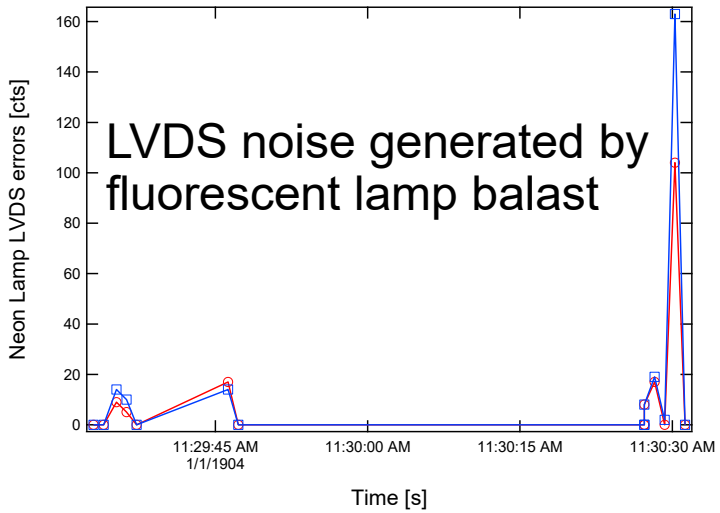
Grounding

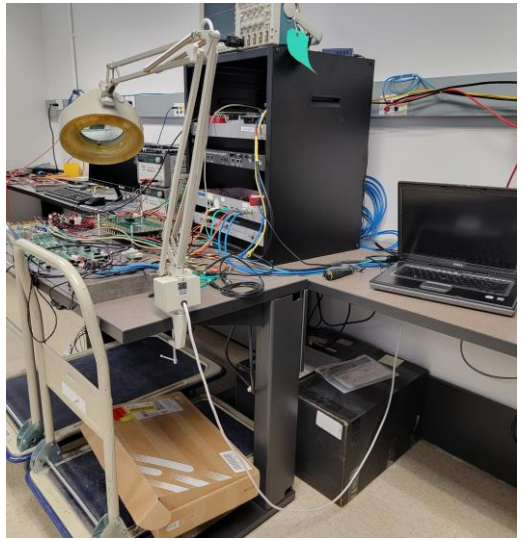
- Test setup

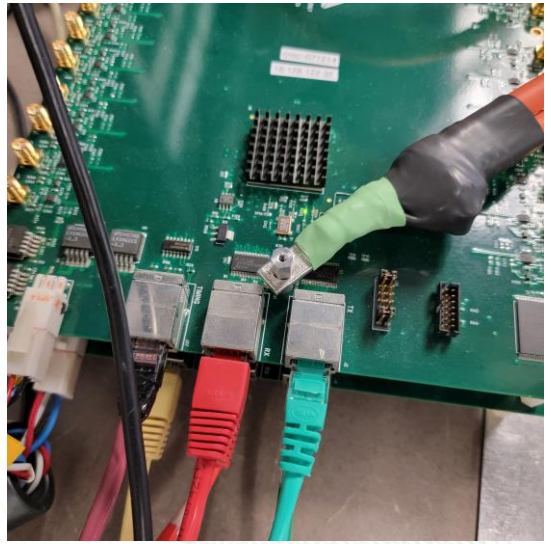






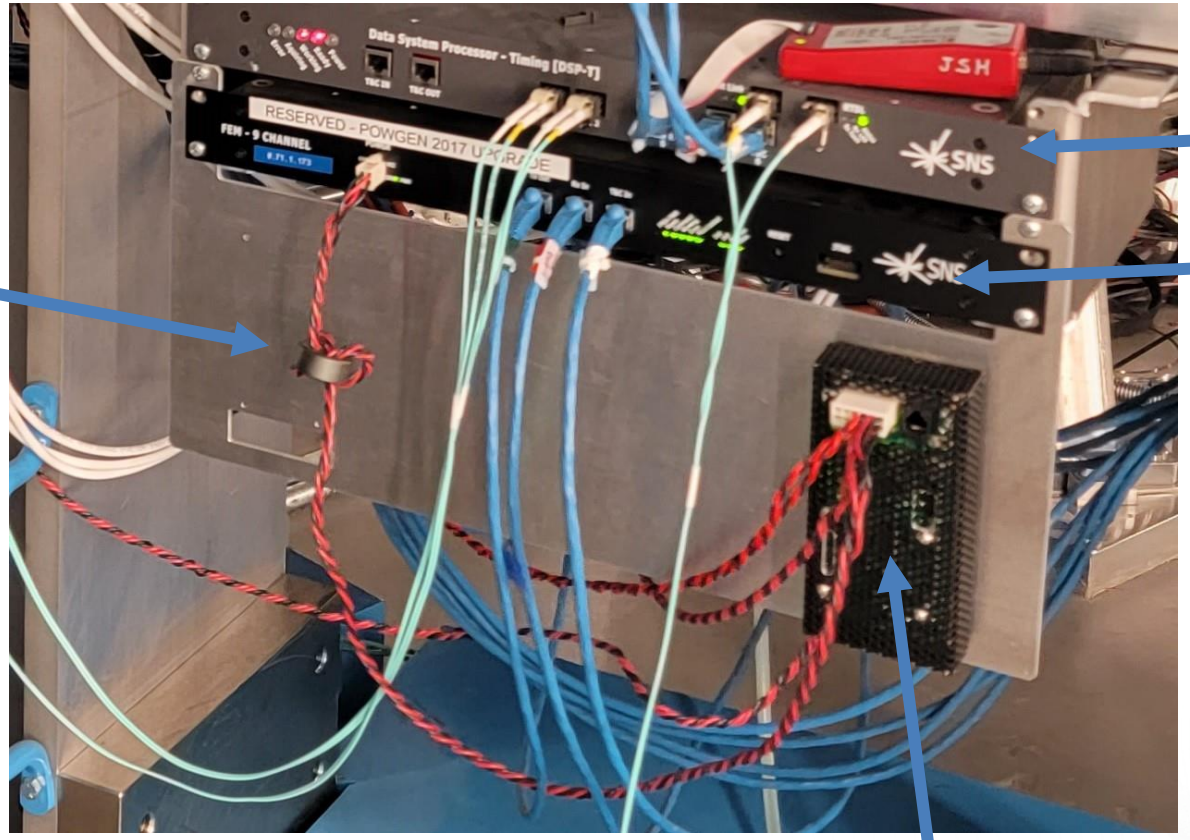






Power Distribution Board (DC-DC conversion)

Toric Ferrite filter

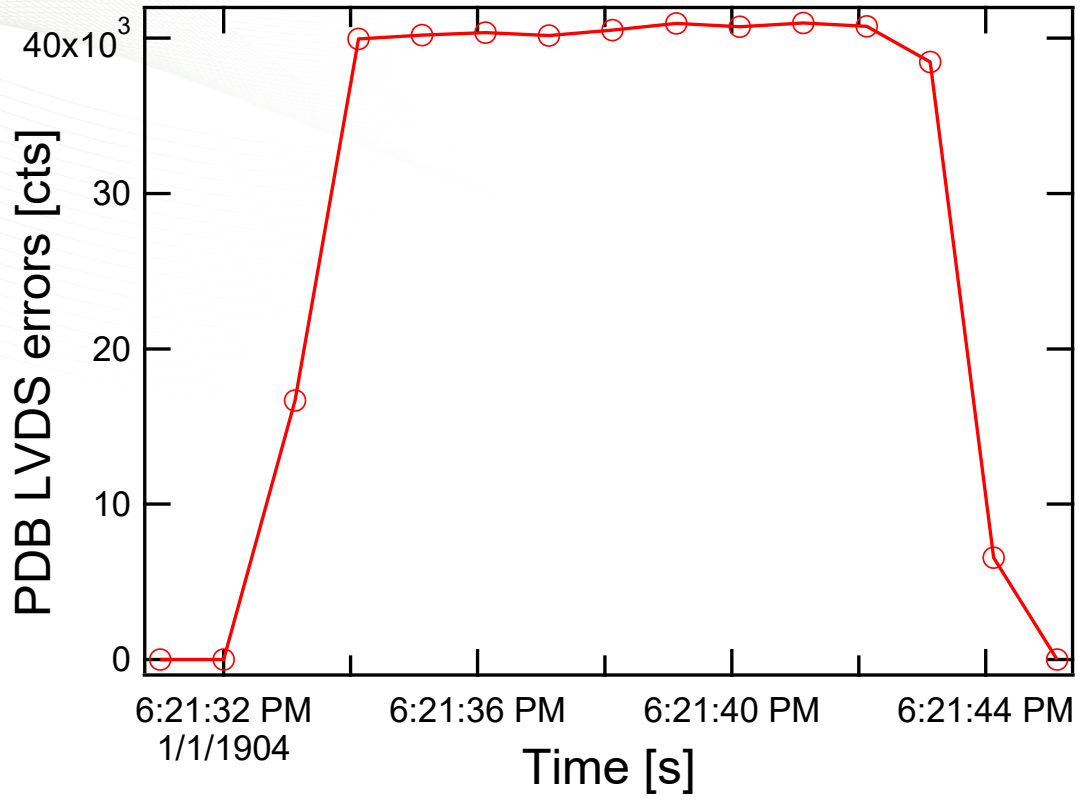


DSP

FEM

PDB DC-DC converters use high frequency conversion circuits to provide regulated DC outputs and input to output isolation where applicable. The frequencies is 300 kHz for our PDB.

Power Distribution Board (DC-DC conversion)

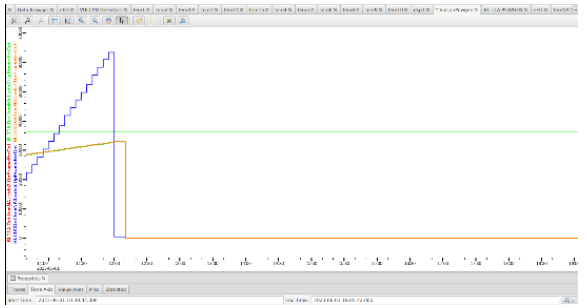


DC to DC converter can become 300 kHz RF antenna driver

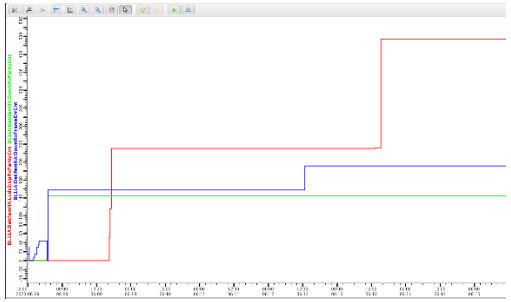
UTP Cat5e cable generates many LVDS errors when the ground (ROC to DSP) is disconnected. The noise signal was generated by attaching a PDB shield to a large 40 × 90 cm metal plate, which behaves as an RF antenna.

Firmware

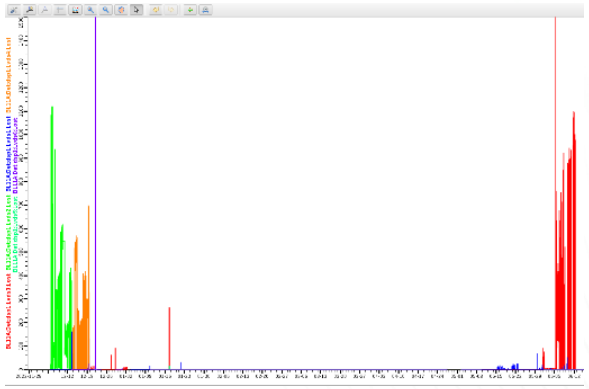
Using side-loaded test FEM firmware to remove known miscounts, no UpFrameErrCnt LVDS errors were observed during a 5 day test run at the beamline.



Parity errors for POWGEN beamline LVDS links.



Many LVDS errors on DSP port connecting to Powgen North FEM chain were observed once in a few months.



Cable upgrade to Cat8

- Firmware

(blue) data cables replaced with Cat8 (white). New cabling has lengths as short as possible.
POWGEN beamline at SNS.

Summary

- Use short cables to minimize skew, signal voltage decrease, dispersion (reduced rise time)
- Adjust skew between pairs at receiver – being developed
- Increase signal transmit – if possible.
- Cable resistance at RF frequencies is much larger than DC resistance, due to skin effect conduction.

Acknowledgements

- Bogdan Vacaliuc,
- Rob Knudson IV,
- Steve Hicks
- Starra Lyons and Charles Ndo for help with the cabling upgrade of POWGEN beamline.

Questions ?