



# Research and Development of the Fast Orbit Feedback System for HEPS

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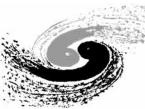


CSNS, DONGGUAN

~ 2250 km →



HEPS, BEIJING

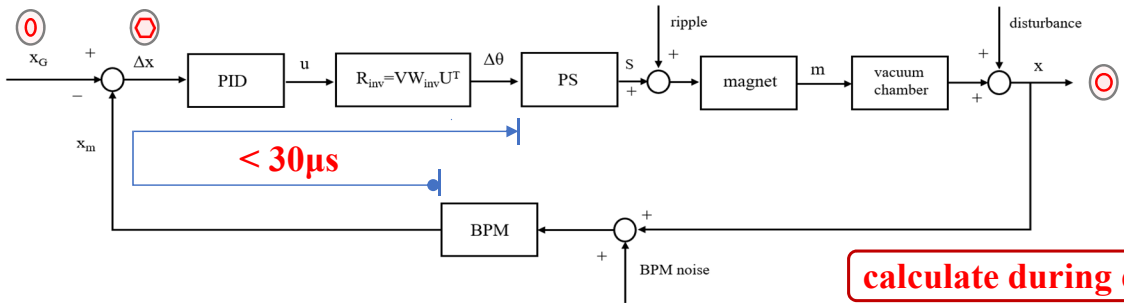


# Fast Orbit Feedback System for HEPS

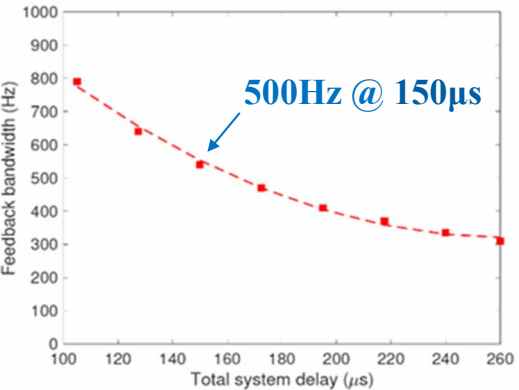
close collaborators: Physics, BPM, Power Supply, Magnet, Vacuum, RF, TM, Control

## Physical requirement(SR: 1360.4 m)

- **Time** : Orbit distortion < 10%(RMS), FOFB delay < 30μs
- **Frequency** : Closed-loop bandwidth >= 500Hz



calculate during data transfer



The response matrix R satisfies:

$$R \Delta\theta = \Delta x = x_m - x_G$$

$$\Delta\theta = R_{inv} \Delta x$$

$\Delta x$  : orbit error given  
 $\Delta\theta$  : corrector strength change  
 $R_{inv}$  : **SVD** inverse response matrix

Fast corrector power supply setting value:

$$S = P\Delta\theta + S_D$$

$S_D$  : corrector DC current

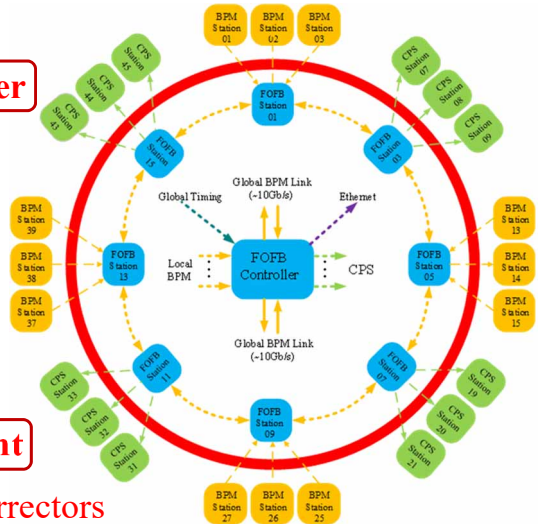
Point-to-Point

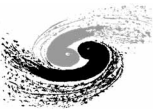
✓ 16 FOFB cells @ 1152 BPMs data @ 384 fast correctors

## Two key issues:

- How to reduce the latency?  
Long time stability and reliability.
- How to maintain the accuracy?  
High performance.

✓ Bi-direction data transfer with each direction 3 channels



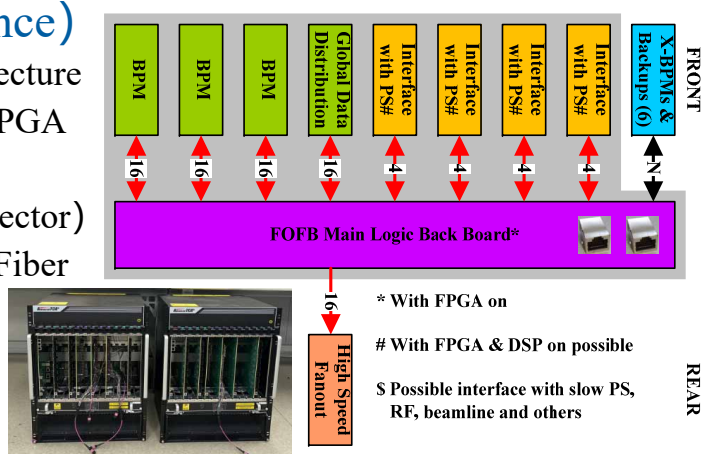


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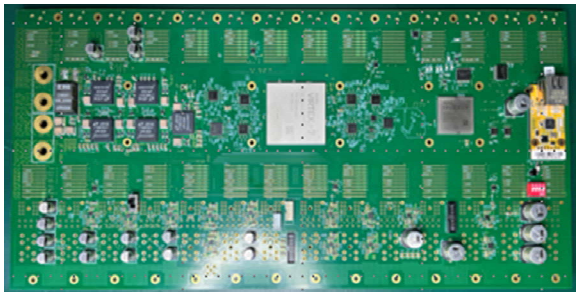
## ● Hardware design (budget & performance)

- ATCA Mechanical architecture
- Core: Xilinx V7 + K7 FPGA
- Interface: Muti-boards (BPM, TM, Fast corrector)
- data trans : Muti-Mode Fiber GTH (4.76Gbps)
- X-BPMs / RF backup
- ... ..

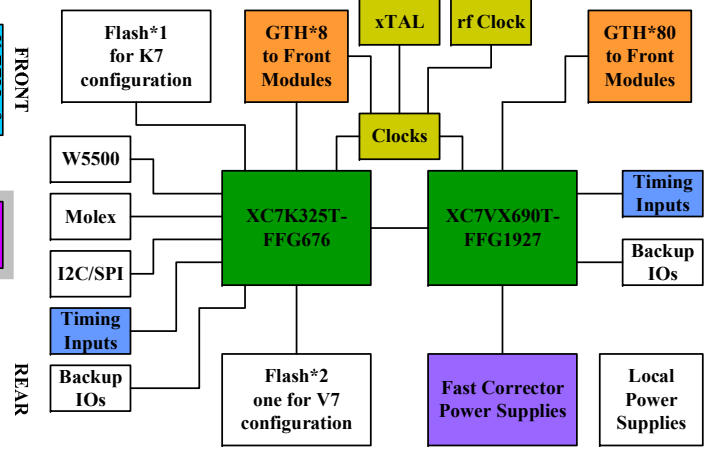
original intention: self-developed and multi-purpose, FOFB、FPS、Timing



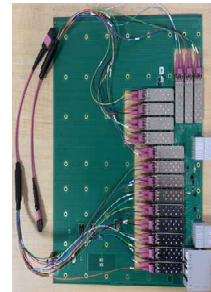
the architecture of Sub-station



Core backplane



the function of core backplane



Interface boards

## ● Hardware finalized (1/4 sub-station)

- Core backplane
- BPM interface board
- Fast-corrector interface board
- Timing interface board



# Fast Orbit Feedback System for HEPS

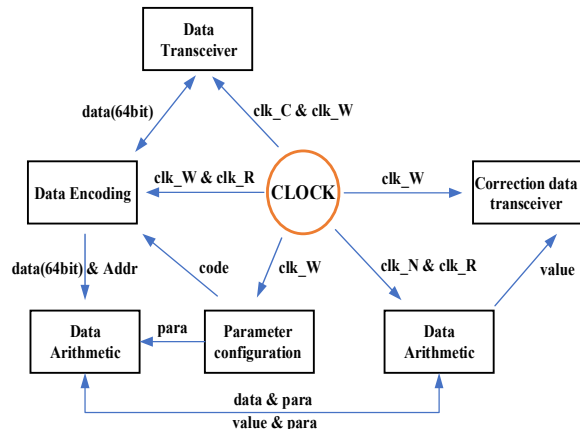
strategy: synchronized with the same clock source, ordering data, interrupt ID and FIFO

## Logic design(modularity)

- A **synchronous** clock  
reduce latency and minimize resources
- The **pipeline**  
make full use of the data transmission delay
- Data width of calculation gradually increased  
to maintain precision



- Clock
- Data encoding
- Data storage
- Data arithmetic
- Data transceiver
- Parameter configuration
- Correction data transceiver



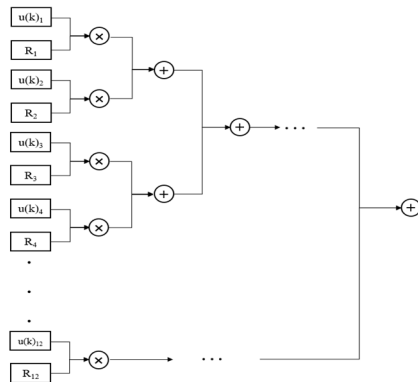
## PID & Matrix multiplication(DSP48E1,3600 slices; BRAM,53Mb)

The equation of incremental PID algorithm :

$$u(k) = u(k-1) + \Delta u$$

$$= u(k-1) + K_p[e(k) - e(k-1)] + K_i e(k) + K_d[e(k) - 2e(k-1) + e(k-2)]$$

- read 12 BPM data and 12 data mapped in the response inverse matrix (24 groups) in one pipeline cycle
- use the "binary tree" to add up the results of the  $12 \times 12$  vectors to get 24 vectors in turn.



BPM	24		
↓ 增加 3			
PID e(k)	27	×	PID 系数 29
↓			
u(k)	56	×	矩阵 29
↓			
S	85		
↓ 增加 5			
θ	90		
↓ 增加 6			
Σθ	96		
↓ ff			
p	32		



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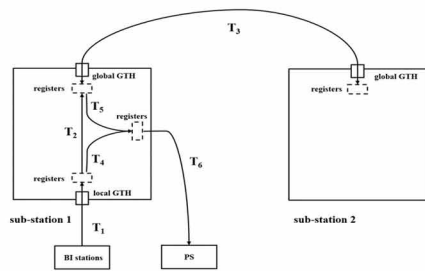
## Time consumption and performance : meeting the requirements (~50% resources used)

- BPM data acquisition: T1
- BPM data treatment: T2
- BPM data transmission: T3
- Matrix calculation for local BPM: T4
- Matrix calculation for global BPM: T5
- Fast-corrector data transmission: T6

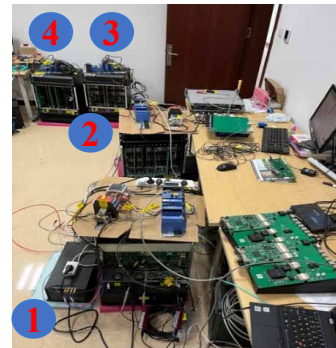
$$T_{total} = T_1 + T_2 + 8T_3 + T_5 + T_6$$

$$T_4 < T_2 + T_3$$

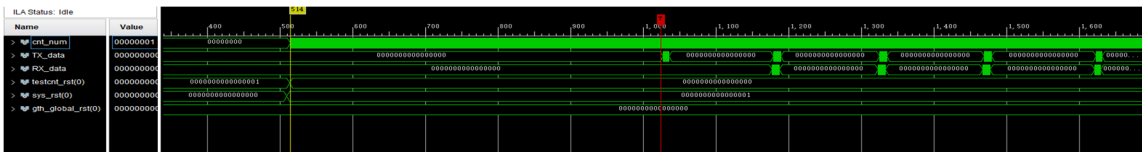
$$T_5 < T_3$$



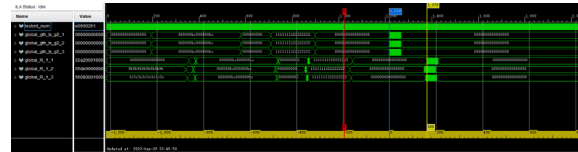
	T <sub>1</sub>	T <sub>2</sub>	T <sub>3</sub>	T <sub>4</sub>	T <sub>5</sub>	T <sub>6</sub>
延时	821ns	705ns	950ns	874ns	773ns	620ns



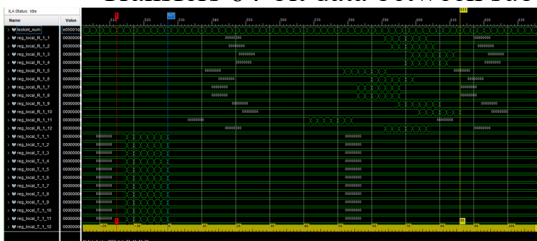
**Total consumption : ~10.5μs**



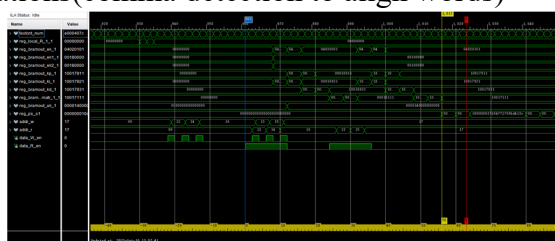
Transfers 64-bit data between sub-stations(comma detection to align words)



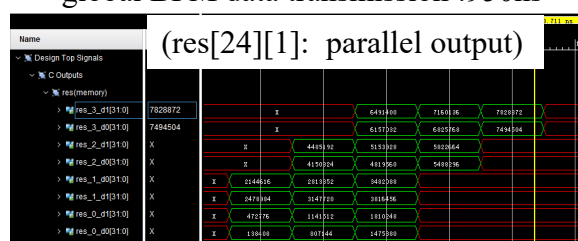
global BPM data transmission :950ns



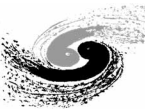
local BPM data transmission :850ns



Pipeline : 470ns



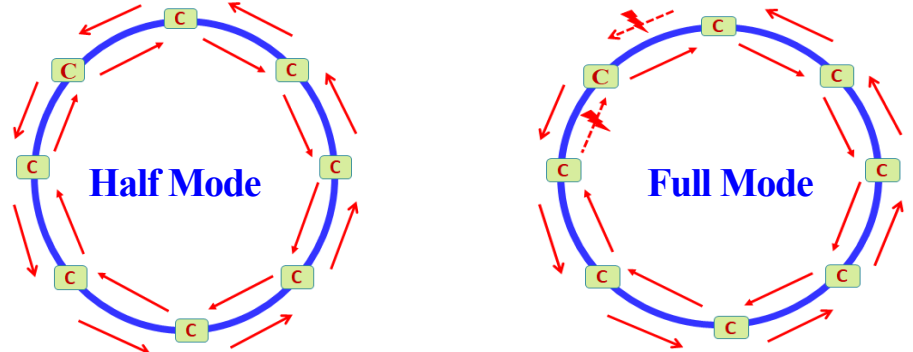
Matrix operation(cell): 53ns



# Fast Orbit Feedback System for HEPS

## • Half ring mode or full ring mode

- normal:  
the data only transfer half a ring
- if disconnection:  
part of data transfer the whole ring

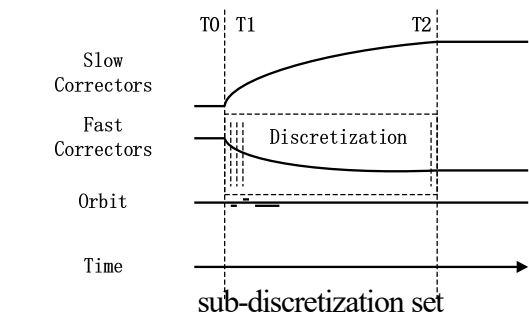
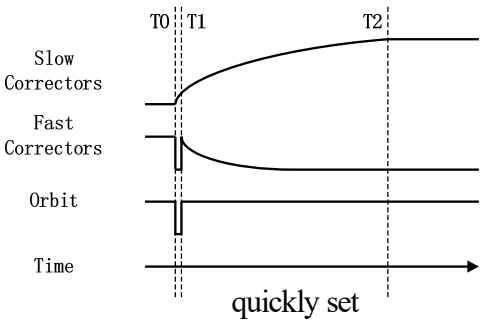
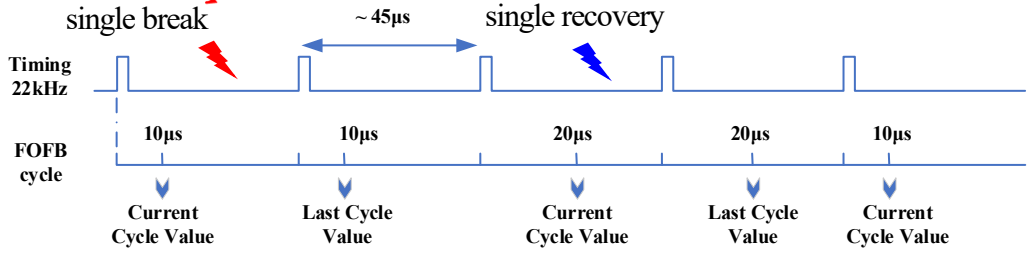


The correction settings does not change much between two adjacent cycles (PID)

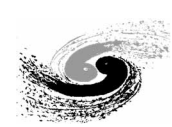
## • Synchronized orbit correction

- Local orbits may not be well corrected by the FOFB due to the slow drift and few fast correctors
- Both fast and slow correctors used for orbit correction, settings synchronized to minimize disturbances

**synchronization!**







# Fast Orbit Feedback System for HEPS

## Summarize

- ✓ All hardware for the 4 sub-stations manufactured, installed and tested;
- ✓ Main logic design finished, further development and test on going.
- ✓ The overall delay is about 10 $\mu$ s, fulfilling the requirements.

**Thanks for your attention !**

