FRIB BEAM RAMP PROCESS CHECKER AT CHOPPER MONITOR

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ICALEPCS 2023 THMBCMO26 Talk Outline

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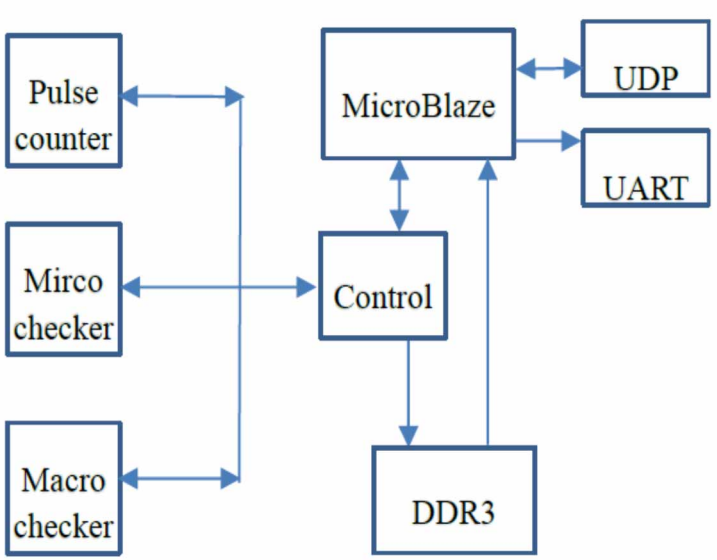
Introduction

- Chopper in the low energy beam line is a key element to control beam power in FRIB. an FPGA-based chopper monitoring system was developed to monitor the beam gated pulse at logic level, deflection high voltage level, and induced charge/discharge current levels, and shut off beam promptly at detection of a deviation outside tolerance.
- Once FRIB beam power reaches a certain level, a cold start beam ramp mode in which the pulse repetition frequency (PRF) and pulse width are linearly ramped up becomes required to mitigate heat shock to the target at beam restart.
- Chopper also needs to generate a notch of 50 μs where no beam is allowed followed by a 9.95 ms period of time where beam is allowed and ramping occurs.
- PRF may ramp up in steps due to requirement of beam current monitor.
- How to monitor such ramp up pulses becomes a big challenge in FPGA design.

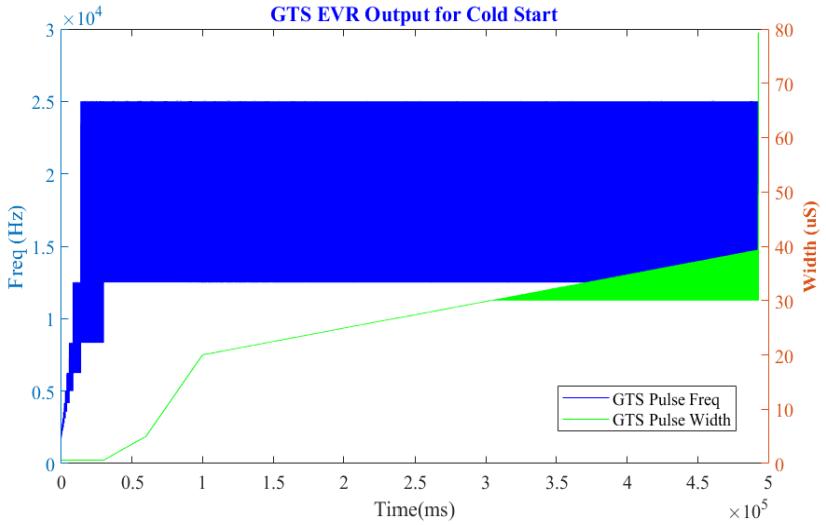
Design

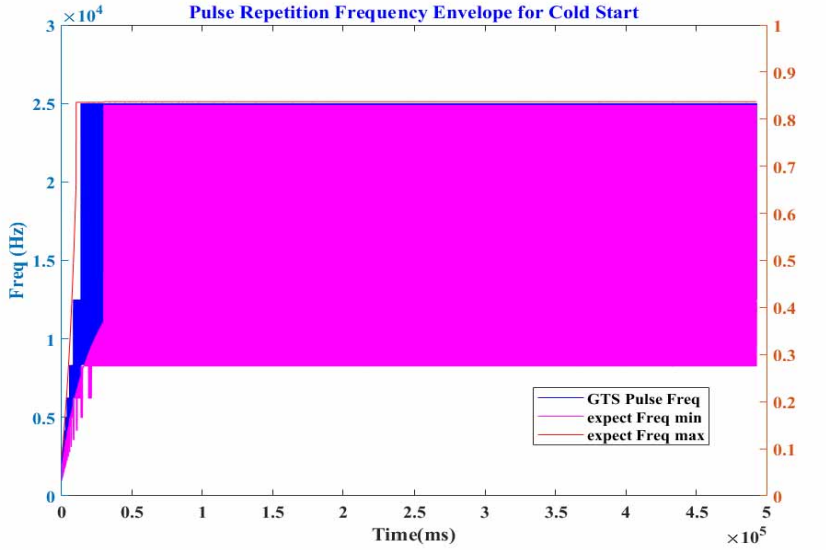
- The design consists of pulse counter, micro checker, macro checker, control, Double Data Rate memory (DDR3), microBlaze and physical interface of User Datagram Protocol (UDP) and universal asynchronous receiver / transmitter (UART). where micro and macro checker ccalculate the range of expected counts of pulse and Beam on Time (BT) of machine cycle respectively ahead of time and check if the presented counts fall out of range.
- Look ahead logic is implemented in micro checker which handles the last two pulse expected range at the end of machine cycle.
- A simplified math model suitable for multi-ramp stages was built for macro checker to calculate expected range of accumulated BT within a given machine cycle.



Test and Results

- The DSPs of micro and macro checker were tested in functional and post route simulations. The timing is checked in the post route simulation. The calculation accuracy is checked in the function simulation of the entire ramp process by comparing the calculation results of DSP with the math result from the test bench.
- A lab test was conducted to test the entire FPGA design. The pulse source is the GTS pulse generator. The results are checked with chipscope and by plotting the measured data stored in DDR3 and readout though UART port. All test results meet the design expectations.
- Plots of the GTS pulse and pulse repetition frequency envelope defined by micro checker is given on the right as an example.





Conclusion

- A beam pulse ramp up process checker system was successfully developed at FRIB which checks the cycle time and PW of every pulse and BT time counts of every MC at the same time.
- The future plan is to integrate the design with other beam mode logics of chopper monitor and the new IOC to be able to read out the process data though UDP channel more quickly.

Questions? You are very welcome toTHMBCMO26 Poster