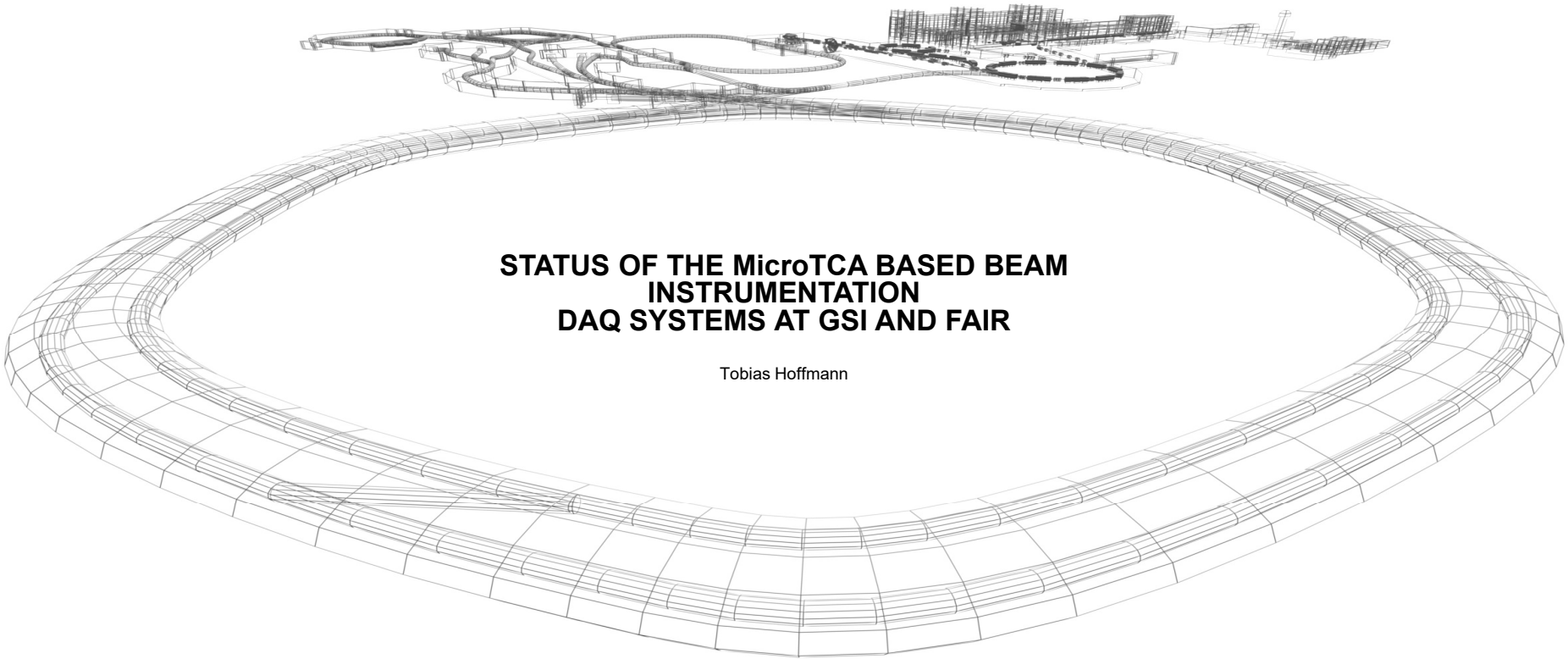


STATUS OF THE MicroTCA BASED BEAM INSTRUMENTATION DAQ SYSTEMS AT GSI AND FAIR

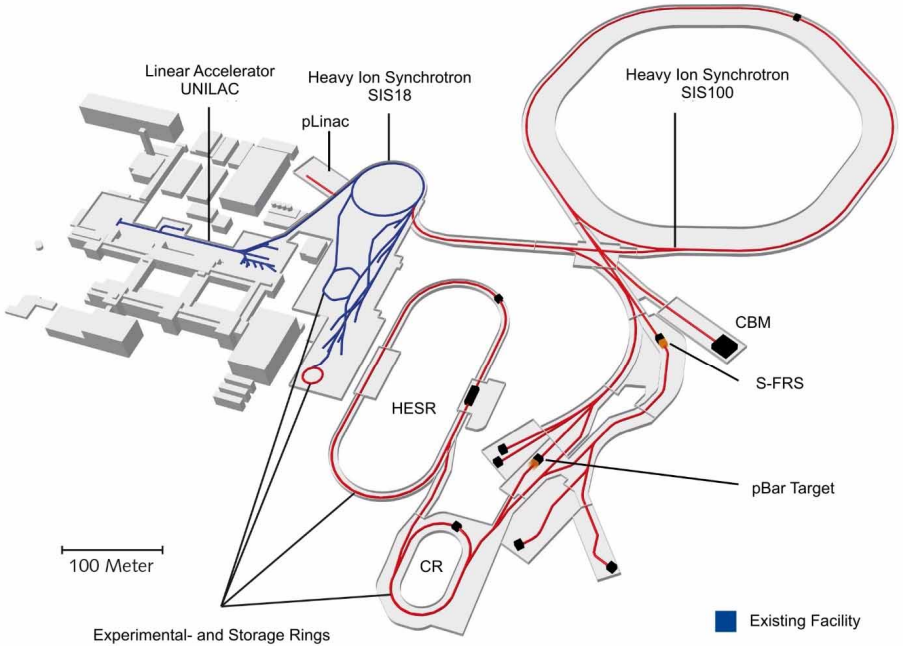
Tobias Hoffmann

Agenda: MicroTCA at GSI and FAIR

1. GSI and FAIR
2. Motivation for MicroTCA
3. Examples of BI DAQ systems (FPGA/FMC based)
   - CRYRING@ESR BPM System
   - Fast Current Transformer (2.5GSPS)
   - Resonant Transformer
   - UNILAC UNIMON System (Online RF status observation)
4. Conclusion and Acknowledgements

Foto: © D. Fehrenz, GSI/FAIR

GSI and FAIR



www.fair-center.eu

primary beams:
up to 35 GeV/u Uranium
up to 90 GeV/u Protons

secondary beams:
- broad range of radioactive beams
- (antiprotons 0 - 30 GeV)

storage and cooler rings:
- radioactive beams
- (10^{11} stored and cooled 0.8 - 14.5 GeV antiprotons)

- very high diversity
- all elements from p to U
- parallel beam operation

What is MicroTCA?

MicroTCA is a:

- form factor like VME, PXI, VXS, VPX, CompactPCI……
- standard (here MTCA.4 from PICMG)

MicroTCA consists of:

- Chassis/Crate (e.g. 6 or 12 slots)
- Power Modules
- Cooling Units
- MTCA Carrier Hub (MCH) as crate controller (IPMI)
- AMCs (Advanced Mezzanine Cards): Compute and I/O modules that plug into the chassis. For example: ADC, Scalers, FMC carriers etc
- JTAG Switch Module (JSM)

Why MicroTCA?

Requirements:

- Higher data bandwidth on backplane
- Modularity (including power supply and fan trays), scalability
- Extensive possibilities for remote maintenance
- High availability / Redundancy
- State-of-the-art bus systems like PCIe (3rd Gen. or higher)
- Availability of measurement boards, such as ADC, counter, I/O or carrier boards for other standard mezzanine technologies, e.g. FMC.

Advantages:

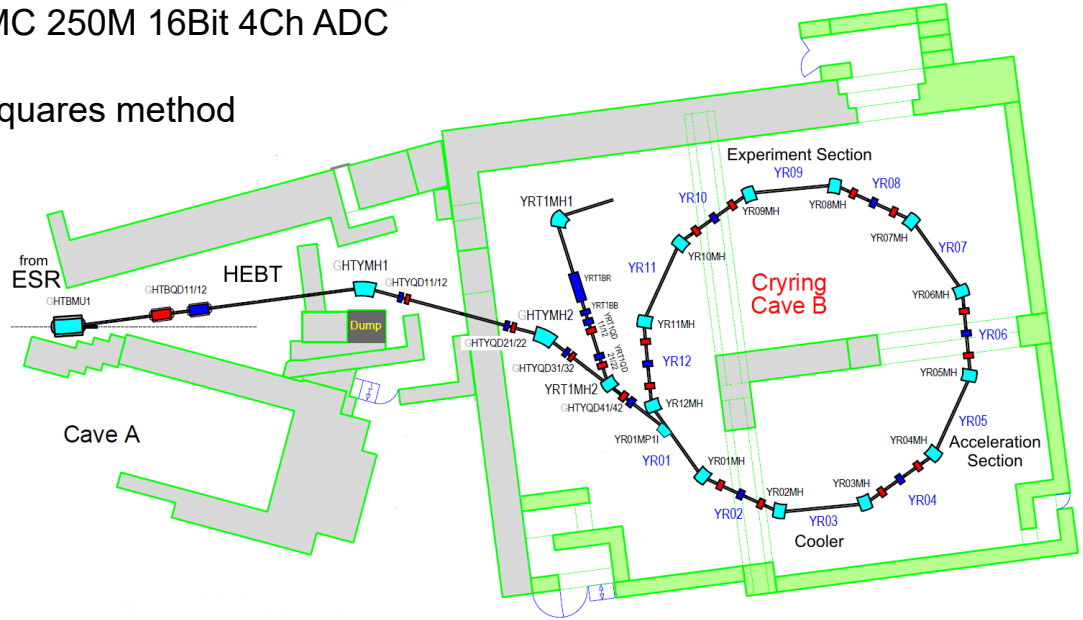
- Huge HEP Community (DESY, ESS, ORNL, LNLS, many others)
- Very active distributors and manufacturers

CRYRING@ESR BPM System

CRYRING@ESR:
- Inkind contribution Sweden (MSL, Stockholm)
- Test accelerator for FAIR concepts and systems (e.g. DAQ)
- 1st Open Hardware Project: AFC V3.1, FMC 250M 16Bit 4Ch ADC
- 18 BPMs (9 hor, 9 ver)
- Difference-over-sum method using least squares method

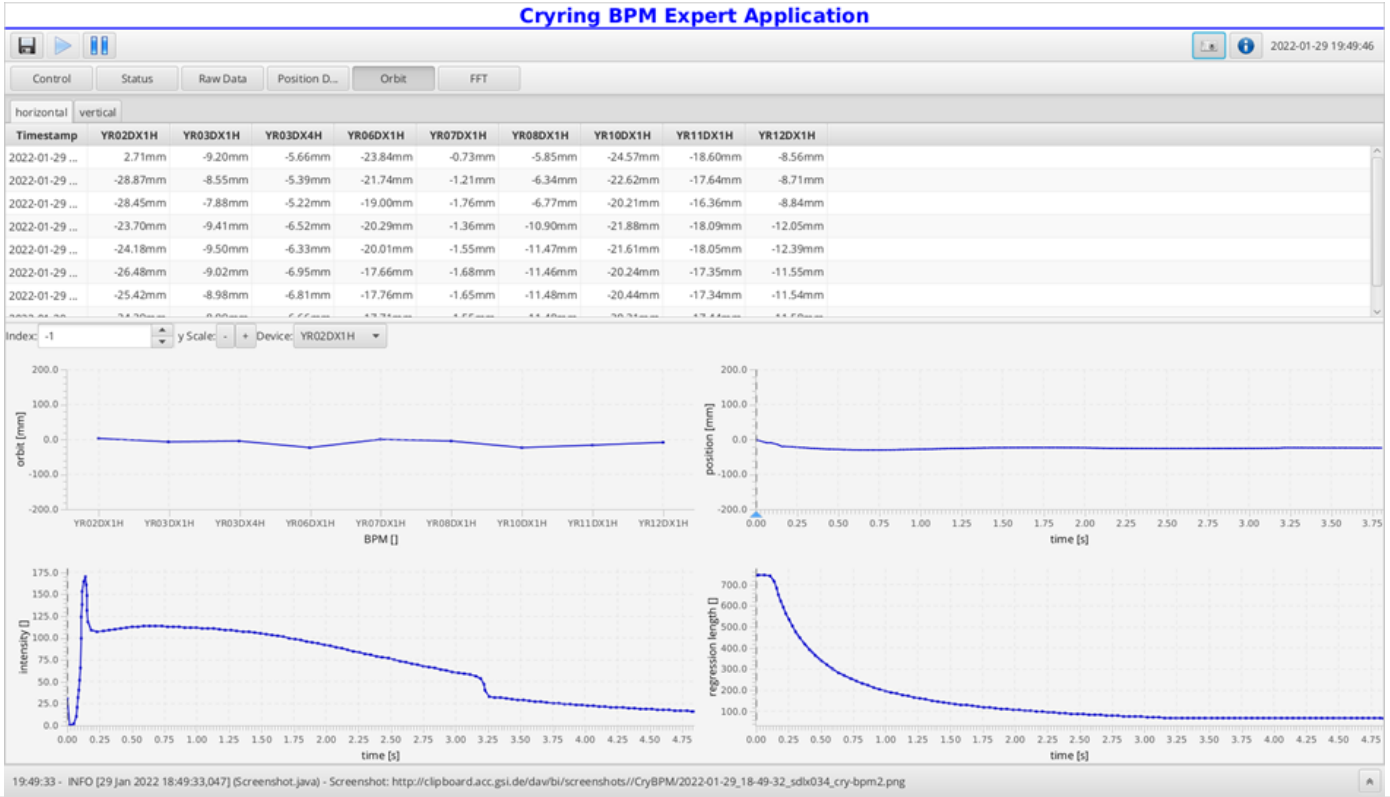
Signal processing (FPGA):
- Raw data @125MSPS
- Chebyshev filter (ion getter pump noise)
- Position calculation (regression fit)
- Running average filter

Signal processing (software, FESA class):
- FFT (Tune)

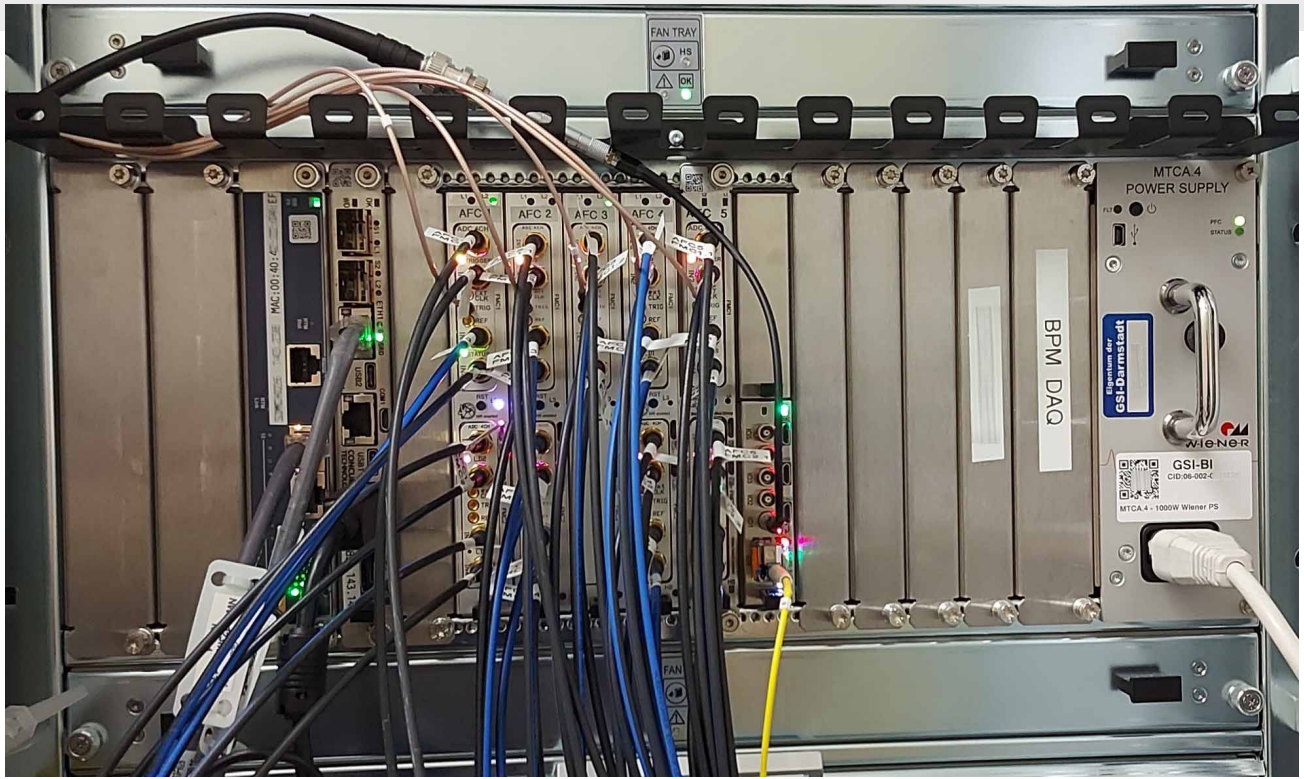


CRYRING@ESR BPM System

Orbit tab with global orbit, BPM intensity (AC power), single BPM position, and fit length (regression)



CRYRING@ESR BPM System



CCT
XEON CPU

AFC with FMC ADC
(OHWR, WUT)

FAIR Timing
Receiver Node

Wiener Power Supply
1000W

Schroff
MTCA.4
Chassis

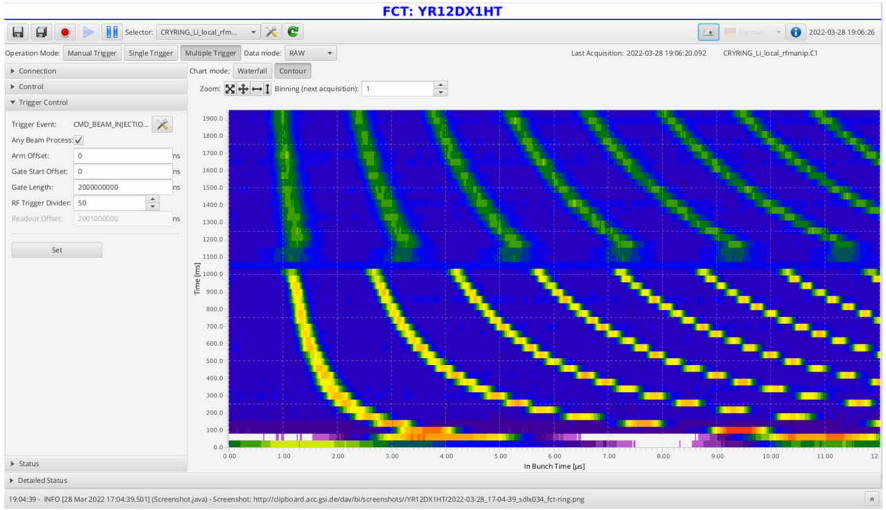
Fast Current Transformer

Operational at SIS18, ESR, Cryring, foreseen for SIS100, HEBT, HESR and CR

Components: SIS8160 + SFMC-AD-2500-14-2 Dual Channel 2.5 GSPS 14-bit Digitizer FMC
SIS8864 64-BIT I/O

Photo: bergoz.com

Bunch dynamics during RF manipulations



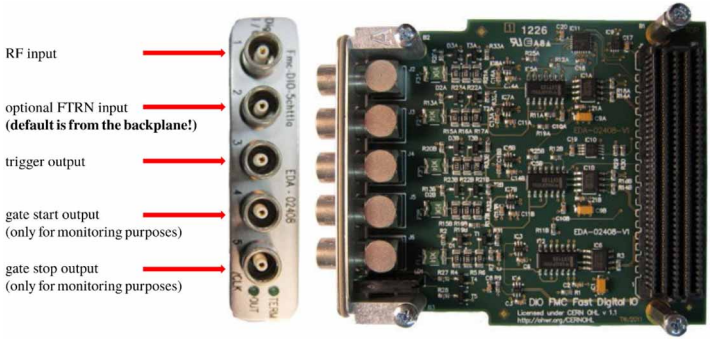
Li^+ beam from local injector over 2 seconds from injection to flattop with rebunching (merge) from h=8 to h=6 in the middle (Cryring)

Fast Current Transformer

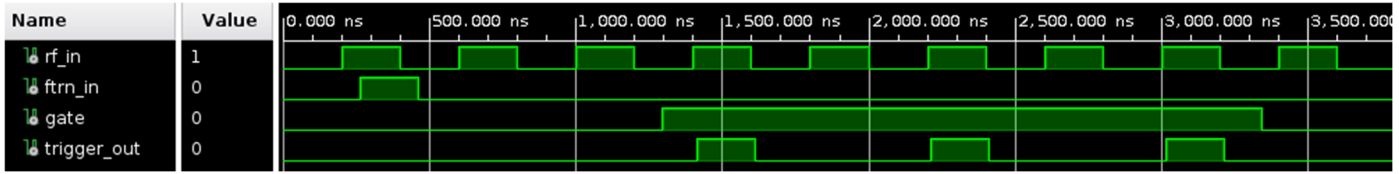
Data acquisition:

- Measure short time periods (few µs) over a longer period using the **multi-event** capability of the ADC
- Measurement time mostly limited by ADC memory
- Measurement triggered by RF pulses
- Trigger rate reduced by **rate divider**

Photo: ohwr.org



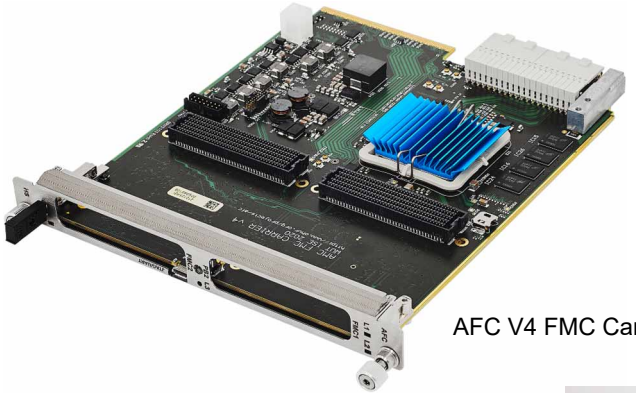
FMC DIO 5CH TTL A on AFC V3.1 as a rate divider



Resonant Transformer

Status: operational
Location: HEBT
Readout: triggered (fast extraction)
max. 2µs bunch length

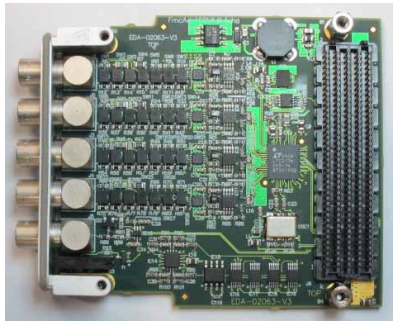
Photos: ohwr.org, LNLS, CERN



AFC V4 FMC Carrier

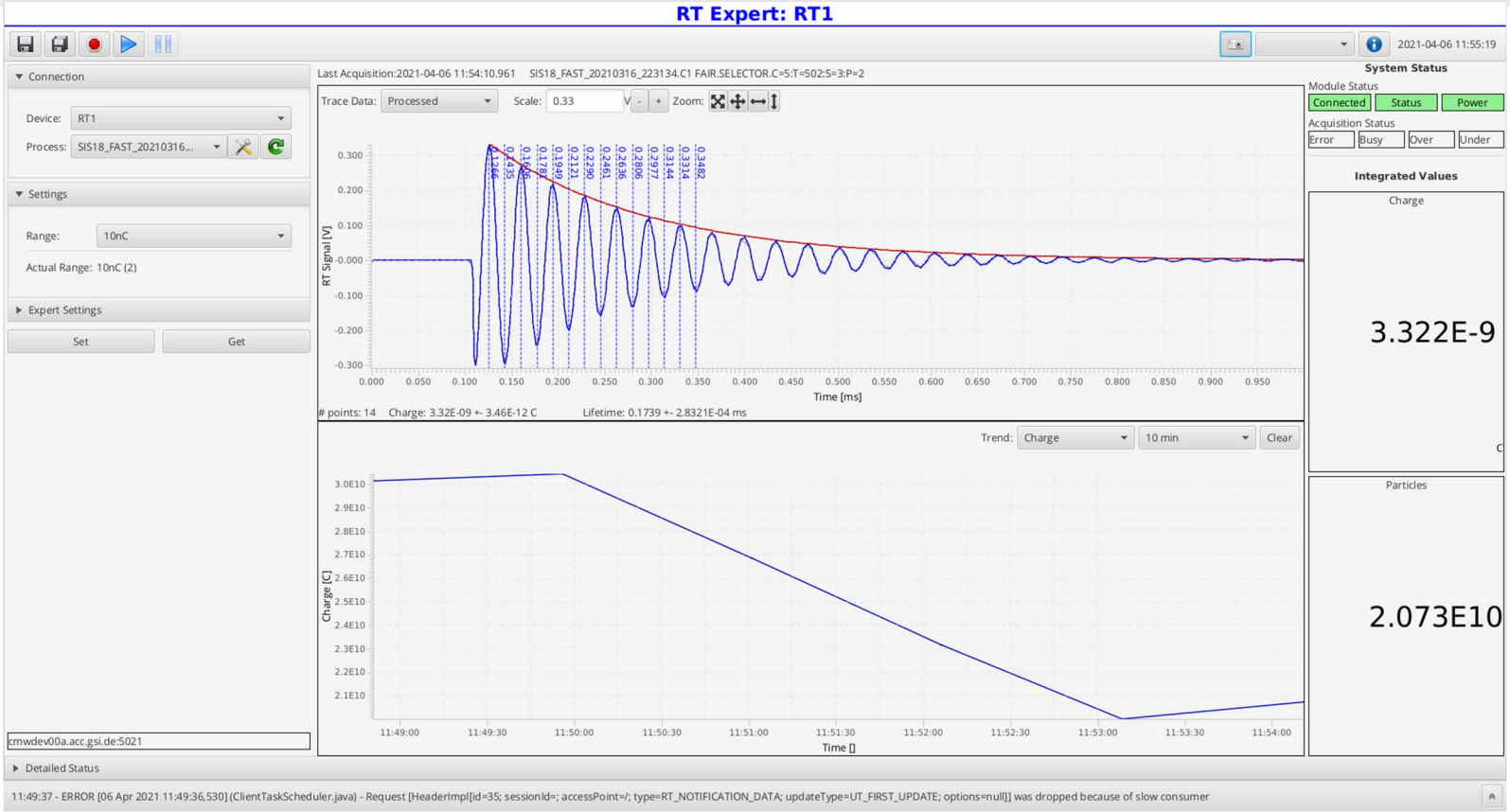
Open hardware project:

- LNLS/WUT development of AFC V4 Carrier
- Firmware integration by LNLS (L. Russo), upgrade to AFC V4 and improvements by R. Geißler
- **Separate configurable triggers via M-LVDS on backplane for each channel**
- OpenMMC



ADC 100MSPS/14Bit

Resonant Transformer



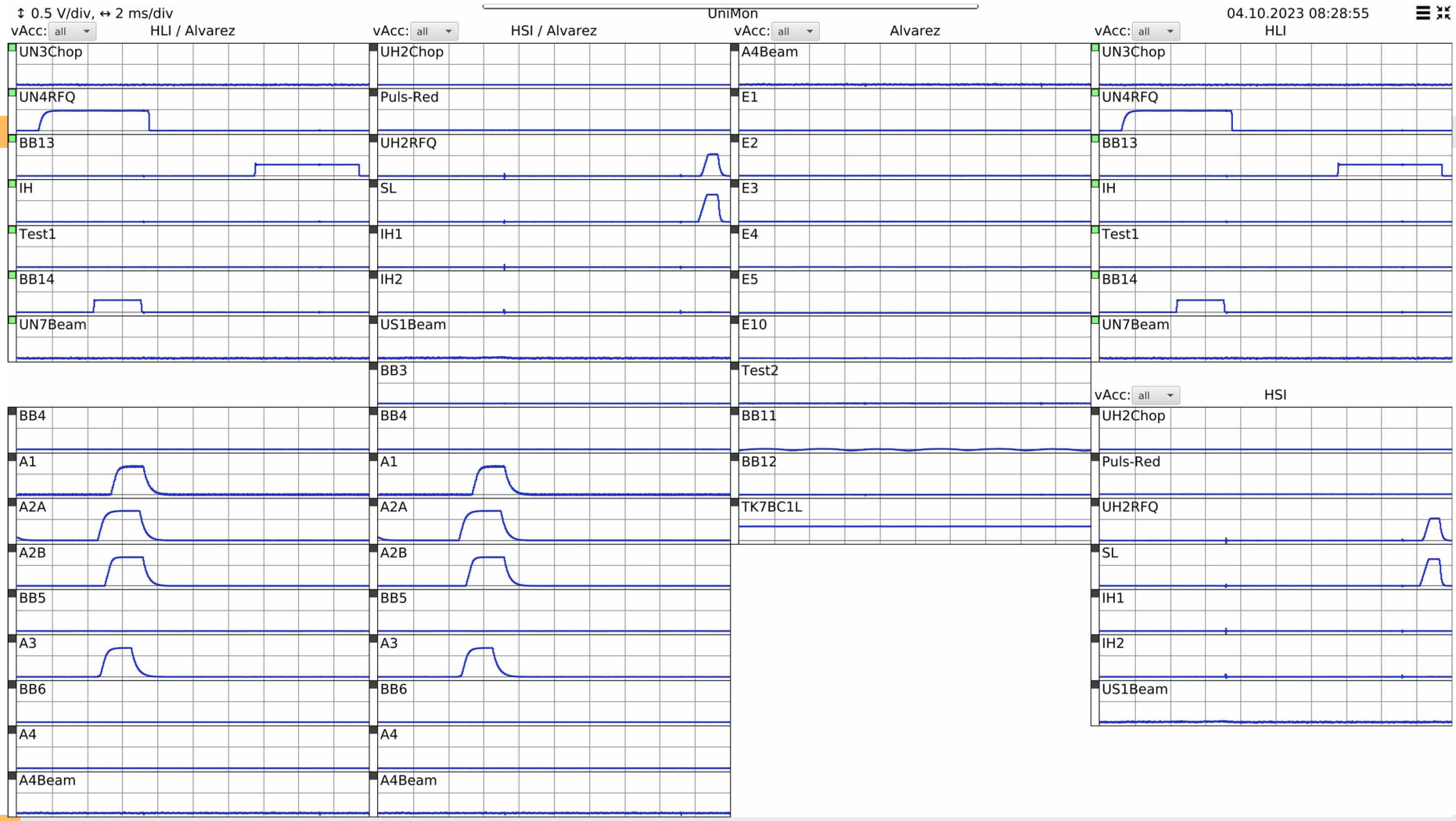
GSI UNIMON (UNILAC rf Monitor)

- Multichannel online display for operating
- Up to 80 channels of UNILAC rf signals
  - buncher, chopper, IH, RFQ and Alvarez
- Triggered readout
- Sample rate of ADCs configurable between 1 kHz and 5 MHz
- WR timing on backplane
- Simple hardware software interface via virtual file access

IOXOS FMC (HPC) ADC_3117:
20 channels ADC 16-bit @ 5 MSPS

Photo: IOXOS

mounted on AFC V4 FMC Carrier (OHWR)


↕ 0.5 V/div, ↔ 2 ms/div
UniMon
04.10.2023 08:28:55
vAcc: all
HLI / Alvarez
UN3Chop
UN4RFQ
BB13
IH
Test1
BB14
UN7Beam
BB4
A1
A2A
A2B
BB5
A3
BB6
A4
A4Beam
vAcc: all
HSI / Alvarez
UH2Chop
Puls-Red
UH2RFQ
SL
IH1
IH2
US1Beam
BB3
BB4
A1
A2A
A2B
BB5
A3
BB6
A4
A4Beam
vAcc: all
Alvarez
A4Beam
E1
E2
E3
E4
E5
E10
Test2
BB11
BB12
TK7BC1L
vAcc: all
HLI
UN3Chop
UN4RFQ
BB13
IH
Test1
BB14
UN7Beam
vAcc: all
HSI
UH2Chop
Puls-Red
UH2RFQ
SL
IH1
IH2
US1Beam

Conclusion

- Using MicroTCA for GSI and FAIR beam instrumentation has proven its worth in daily operation
- MicroTCA covers all needs for GSI beam instrumentation
- The very well equipped backplane, with Ethernet, PCIe, M-LVDS, JTAG lines, and others, offers very many applications in one system
- The openly usable FPGAs, like with OHWR products, allow the best possible adaptation to the DAQ requirements, provided that an FPGA expert is available.
- COTS and OHWR can go together

Acknowledgements

Greatest thanks to:

- the colleagues from CERN BE-CEM/CCS for many years of inspiration in software and hardware concepts, in particular, we would like to acknowledge the introduction of the CERN Open Hardware License.
- DESY for the valuable workshops, tutorials and support around MicroTCA.
- the many supporting industry partners such as:

  Struck (SIS), Powerbridge, Tews, Emcomo, NAT, IOXOS, Wiener and Schroff.

Questions?

Foto: © D. Fehrenz, GSI/FAIR