Development and Test Operation of the Prototype of the New Beam Interlock System for Machine Protection of the RIKEN RI Beam Factory

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Introduction of RIKEN Radioactive Isotope Beam Factory (RIBF) and its accelerators

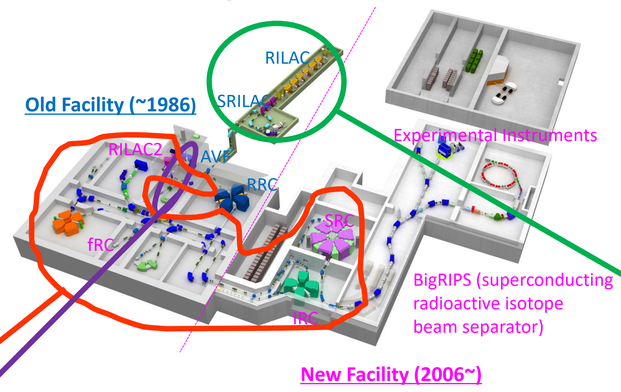
- RIBF is a cyclotron-based heavy-ion accelerator facility for nuclear science.
- Various acceleration modes can be achieved by changing combination of the accelerators used.
- RIBF accelerators can supply RI beams at energies of several hundreds MeV/nucleon over the whole range of atomic masses.

Ex.) 345-MeV/nucleon ^{238}U beam of 117 pnA
345-MeV/nucleon ^{78}Kr beam of 486 pnA

< Accelerators >
- Frequency-variable RIKEN heavy-ion linac (RILAC, 1980)
- K540-MeV RIKEN Ring Cyclotron (RRC, 1987)
- K70-MeV Azimuthally Varying Field Cyclotron (AVF, 1990)
- K570-MeV Fixed frequency Ring Cyclotron (fRC, 2006)
- K980-MeV Intermediate stage Ring Cyclotron (IRC, 2006)
- K2600-MeV Superconducting Ring Cyclotron (SRC, 2006)
- New linac injector (RILAC2, 2010)
- Superconducting RIKEN linear accelerator (SRILAC, 2020)

< Research Activities >
- Nuclear Physics Research
- Discover of New Elements
- Applied Research (Radiation Biology, RI Applications)

<Bird's Eye View of RIBF>



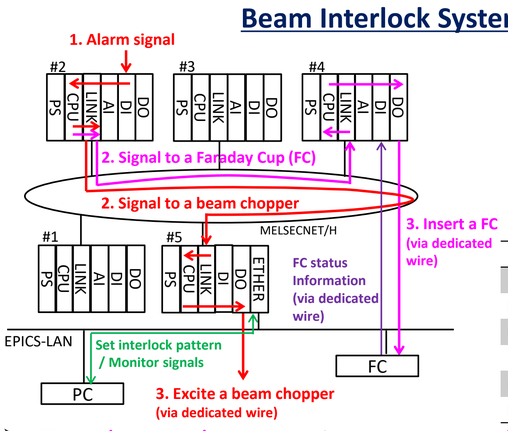
<Control System>
- Components of the RIBF accelerator complex are controlled by EPICS, with a few exceptions (RF systems, etc.).
- All the essential operation datasets of EPICS and other control systems are integrated into the EPICS-based control system.
- Two types of interlock systems :
  - Radiation safety interlock system for human protection
  - Three kinds of beam interlock system for machine protection

<Example of RIBF Components controlled by EPICS>

Components	Amount
Magnet Power Supply	944
Faraday Cup	116
Beam Profile Monitor	186
Vacuum Gate Valve	96

Beam interlock system for machine protection (in operation)

Beam Interlock System (BIS) (2006~)

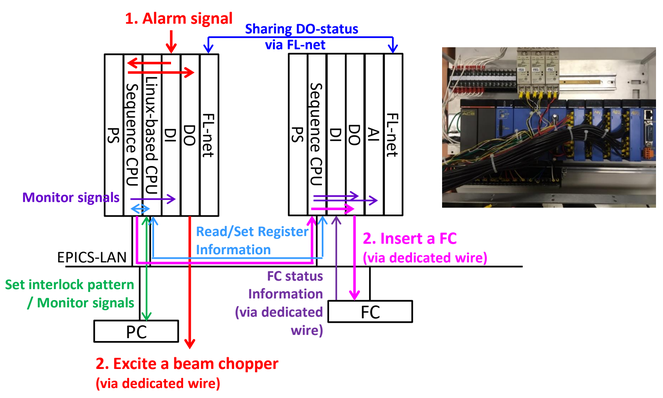


Type	Product	Note
CPU	Q02HCPU	Sequence CPU
DI Module	QX41	
DO Module	QY40P	Transistor contact
AI Module	Q68ADV	
Melsecnet/H Module	QJ71LP21-25	
Ethernet Module	QJ71E71-100	

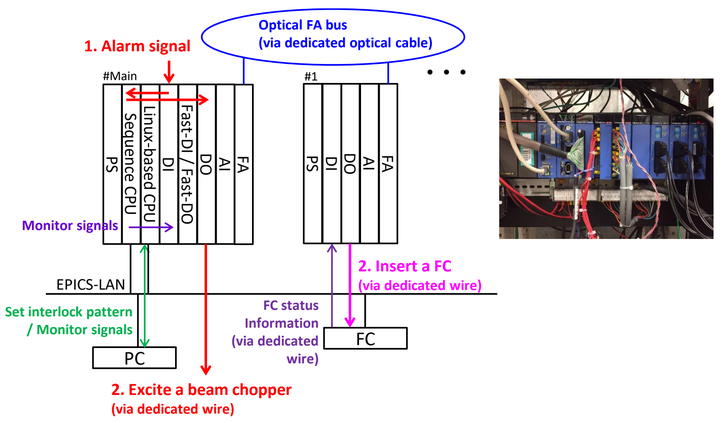
- Based on Melsec-Q series programmable logic controllers (PLCs) (Mitsubishi Electric Corporation), 5-station configuration.
- Stop beams ~ 15 ms after receiving an alarm signal (response time, design value : 10 ms) .
- BIS outputs a signal to one of the beam choppers, which immediately deflects the beam downstream of the ion sources, and also inserts a beam stoppers (Faraday cup) installed upstream of the problematic component.
- Two sets of BIS with the same specifications monitor almost all the components of the RIBF accelerators except the components monitored by AVF-BIS and SRILAC-BIS.
- Total signals of BIS (two sets total) : 768 DI / 224 AI / 160 DO

AVF-BIS (2019~) / SRILAC-BIS (2020~)

AVF-BIS



SRILAC-BIS



- Implements interlock logic equivalent to BIS.
- Based on FA-M3 series PLCs (Yokogawa Electric Corporation).
- Utilizes two different types of CPUs :
  - Sequence CPU : Implement interlock logic (high-speed processing and high reliability are required)
  - Embedded EPICS on Linux-based PLC-CPU : Parameter setting and monitoring the interlock signals

Type	Product	Note
CPU1	F3SP71-4S	Sequence CPU
CPU2 (AVF-BIS)	F3RP61-2L	Linux-based CPU
CPU2 (SRILAC-BIS)	F3RP71-2L	Linux-based CPU
DI Module	F3XD32-3F	
DO Module	F3YD14-5A	Transistor contact
AI Module	F3AD08-1V	
FL-net Module	F3AD08-1V	Transmission speed : 10 Mbps
High-speed DIO Module	F3DF01	Embedded Xilinx Spartan-6 LX FPGA
FA bus module	F3LR02-0N	

[AVF-BIS]
- 2-station configuration, sharing the status of DO via a dedicated FL-net (an open network protocol used for interconnection between controllers).
- Total signals : 64 DI / 24 AI / 28 DO
- Average response time : 2 ms (signal input and output are carried out in the same station) / 5.4 ms (signal input and output are carried out at different stations) .

[SRILAC-BIS]
- 1-main station and 7-substations, communicate via an optical FA bus.
- Total signals : 272 DI / 56 AI / 272 DO
- Implements high-speed I/O module with FPGA in addition to the regular I/O module.
- Average response time : 6 ms (regular I/O) / 78 μs (high-speed I/O)

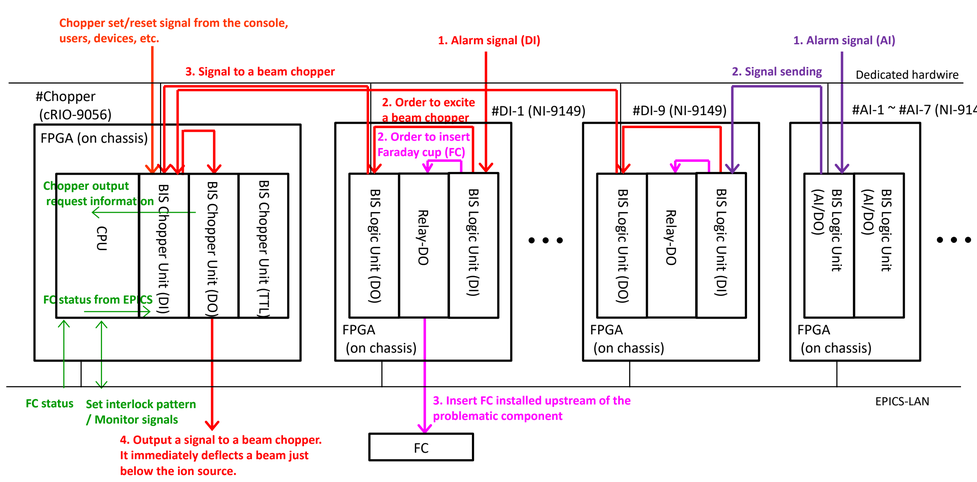
Development the successor system of BIS (RIBF-BIS2)

< System Goals>
Stop a beam within 1 ms after detecting equipment anomaly or excessive beam loss.

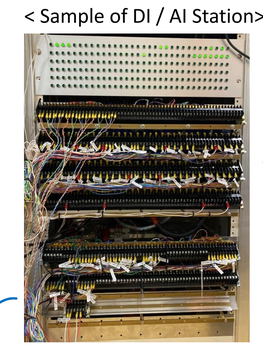
< Basic Design>
- Implement interlock logic equivalent to BIS.
- Based on the CompactRIO (National Instruments)
- Utilizes FPGA layer and RT-OS layer:
  - FPGA : Implement Interlock logic (high-speed processing and high reliability required)
  - RT-OS : Parameter setting and monitoring the interlock signals
- To be installed in the same location as the BIS (exiting signal wiring from each device is to be reused).
- Signals in Each DI Station : 192 DI / 32 DO / 8 Relay-DO (for Faraday cup)
- Signals in Each AI Station : 64 AI / 2 DO
- Signals in Chopper Station : 160 DI / 32 DO / 8 TTL
- Controlled by using EPICS by setting up an EPICS server on the RT-OS.
- GUI for signal settings and monitoring of RIBF-BIS2 has been developed using the Control System Studio (CSS) of EPICS.
- Log system has been developed based on the system used in RILAC operation.

< Improvements from BIS / AVF-BIS>
- Stations dedicated to AI signal processing and stations dedicated to DI signal processing will be installed respectively to respond to the instantaneous signals output from the equipment when an anomaly occurs (digital signal) in the fastest time. When an analog signal sampled at a certain period exceeds a threshold value and is determined to be abnormal, it takes longer than the aforementioned signal. An alert to an AI Station is output as a DO signal from the AI Station, and the DO signal is input t the DI Station via a dedicated wire to stop the beam.
- Combine the two sets of BISs into a single system.

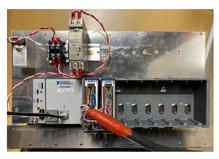
< Development as of Summer 2023>
- 2 DI Stations + 1 AI Station + Chopper Station were installed in a part of BIS with connecting the input signals into the those stations in parallel with the BIS.
- Average response time : 129.0 μs (DI) / 470.3 μs (AI)
  by adding a pull-up circuit (constant current diode (E-183) + LED (DB24-79GS)) in parallel to the signal input part.
- Number of shared variables registered on the EPICS server : 1300 (DI Station + Chopper Station) / 530 (AI Station)



< Sample of DI / AI Station>



DI Station before wiring
(behind the terminal board)



AI Station after wiring
(behind the terminal board)

BIS Logic Unit (BLU) : Judge conditions such as the mask and holding time for each alert signal input and sends a signal to the BCU that requires the excitation of a beam chopper via a dedicated hard wire.
BIS Chopper Unit (BCU) : Compares the input signal from the BLU and the insertion status of the Faraday cup and outputs a signal to the beam chopper when necessary.

<Modules in the Chopper Station>

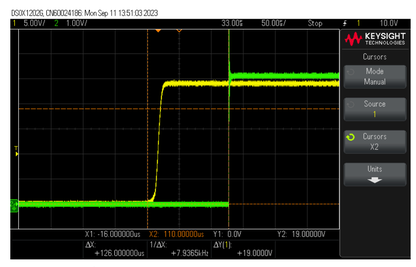
Type	Product	Quantity
Chassis	cRIO-9056	1
DI Module	NI-9426	5
DO Module	NI-9475	1
5V TTL	NI-9401	1

<Modules in the DI Station>

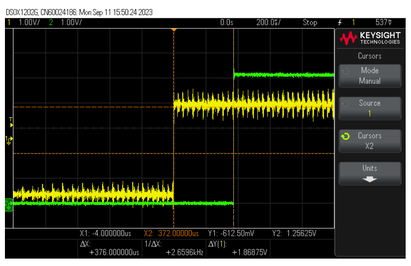
Type	Product	Quantity
Chassis	NI-9149	1
ADI Module	NI-9426	6
DO Module	NI-9477	1
Relay-DO	NI-9485	1

<Modules in the AI Station>

Type	Product	Quantity
Chassis	cRIO-9056	1
AI/DO Module	NI-9205	2



< Signal output timing at DI Station>
Measured by generating signal experimentally from one of the actual components



< Signal output timing at AI Station>
Measured by signal generated by a function generator

* Yellow and green lines show the input and output signals, respectively.

We plan to replace BIS with RIBF-BIS2 within 2 years.