The SILF Accelerator Controls Plan

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Abstract

The Shenzhen Innovation Light Source Facility (SILF) is an accelerator-based multidiscipline user facility planned to be constructed in Shenzhen, Guangdong, China. This poster introduces controls design outline and progress. Some technical plans and schedules are also discussed.

Introduction

The SILF is a fourth-generation medium-energy synchrotron radiation light source that envisions a future with over 50 beamlines. Its primary focus lies in supporting the development of domestic core industries, advancing frontiers in basic science research, and addressing strategic imperatives, including integrated circuits, bio-medicine, advanced materials, and advanced manufacturing.

The accelerator complex is composed of a 200 MeV linac, a booster with ramping energy from 0.2 GeV to 3.0 GeV, and a 3.0 GeV storage ring as shown in Figure 1. Two transport lines are designed to connect the linac, booster and storage ring. The circumference of the storage ring is 696 m, which includes 28 hybrid seven-bend achromat (H7BA) lattice periodic units to achieve the emittance below 100 pm·rad. The top-up operation mode (300 mA, 928 bunches) is considered, and a brightness of about $10^{22} s^{-1} mm^{-2} m \cdot rad^{-2} (0.1\% \text{ bandwidth})^{-1}$ is expected at the photon energy of 10 keV for SILF. Considering machine errors and correction, the dynamic aperture of the storage ring is 7.2 mm, which meets the requirement for off-axis injection. Furthermore, we have placed significant emphasis on the control system, which plays a pivotal role in providing and assuring high availability and reliability, laying a solid foundation for successful user experiments.

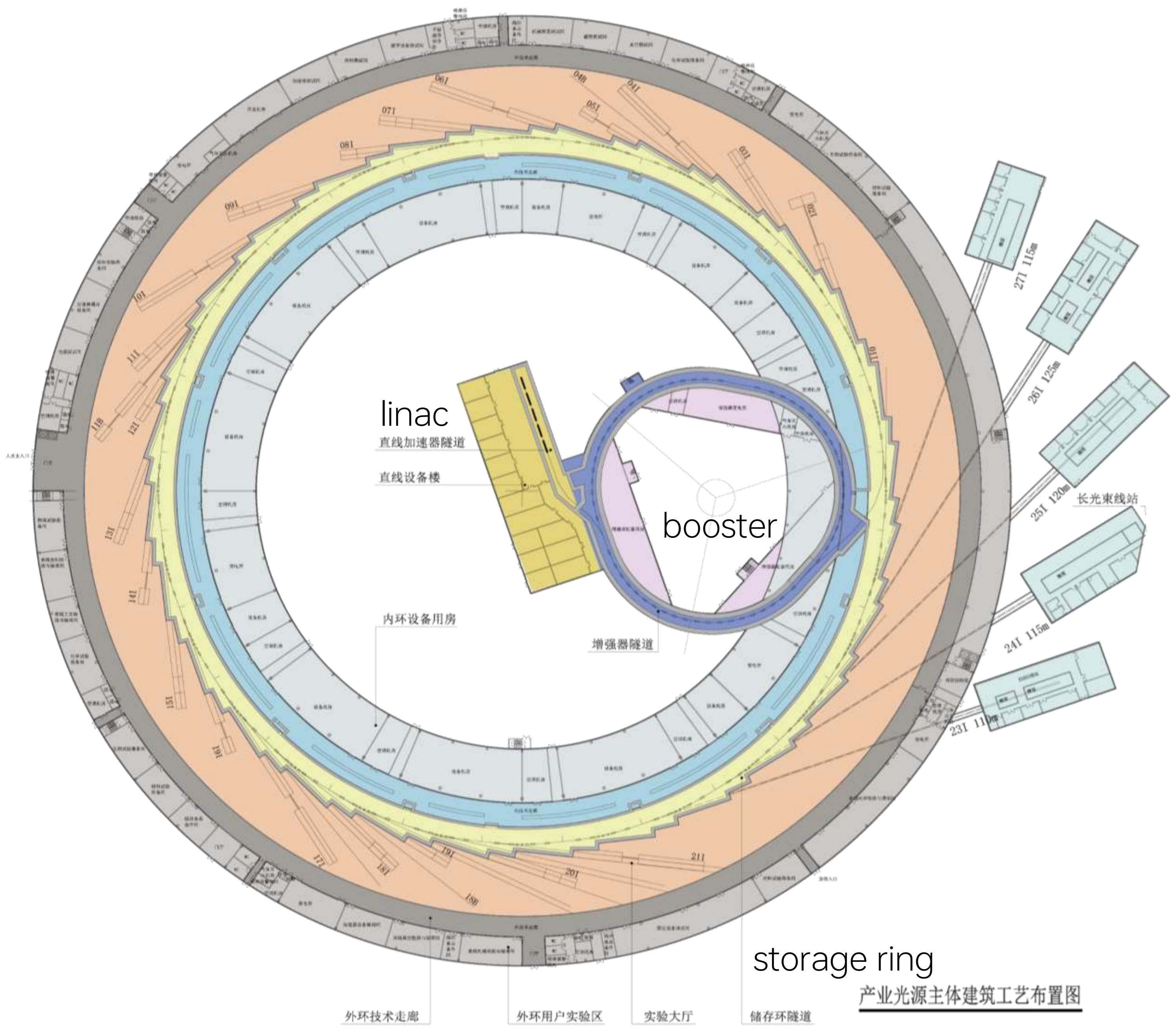

Figure 1 Schematic layout of the SILF project

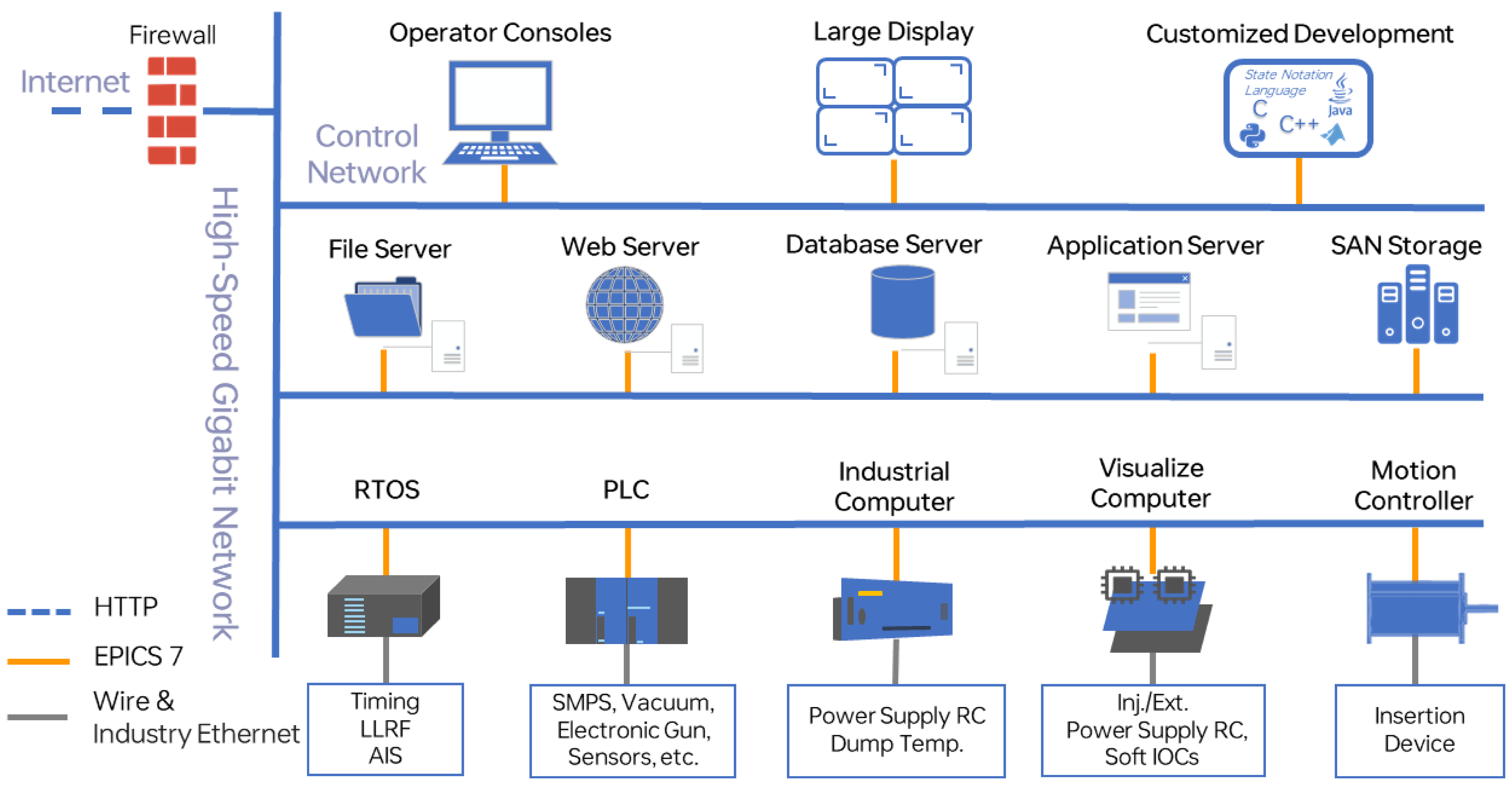

Figure 2 EPICS typical usage model of SILF

Hardware & Software

SILF uses the EPICS family of distributed control system software for the creation of a facility-wide data communication layer, which integrates all technical systems that participate in photon production and experiments. The typical EPICS usage model of SILF is a three-tier system including the presentation layer, the middleware service layer and the frontend device layer as shown in Figure 2.

The accelerator control system comprises a network of interconnected and distributed control and computing systems, serving various control domains and purposes. To ensure optimal performance, we will employ standardised hardware technologies, including MicroTCA, EtherCAT, and common industrial automation technology. Additionally, multiple PLC-based systems will be deployed for equipment interlock and conventional facilities. Industrial computers-based Soft IOCs will facilitate communication with the PLCs via Ethernet/IP, with each IOC featuring precise data timestamping.

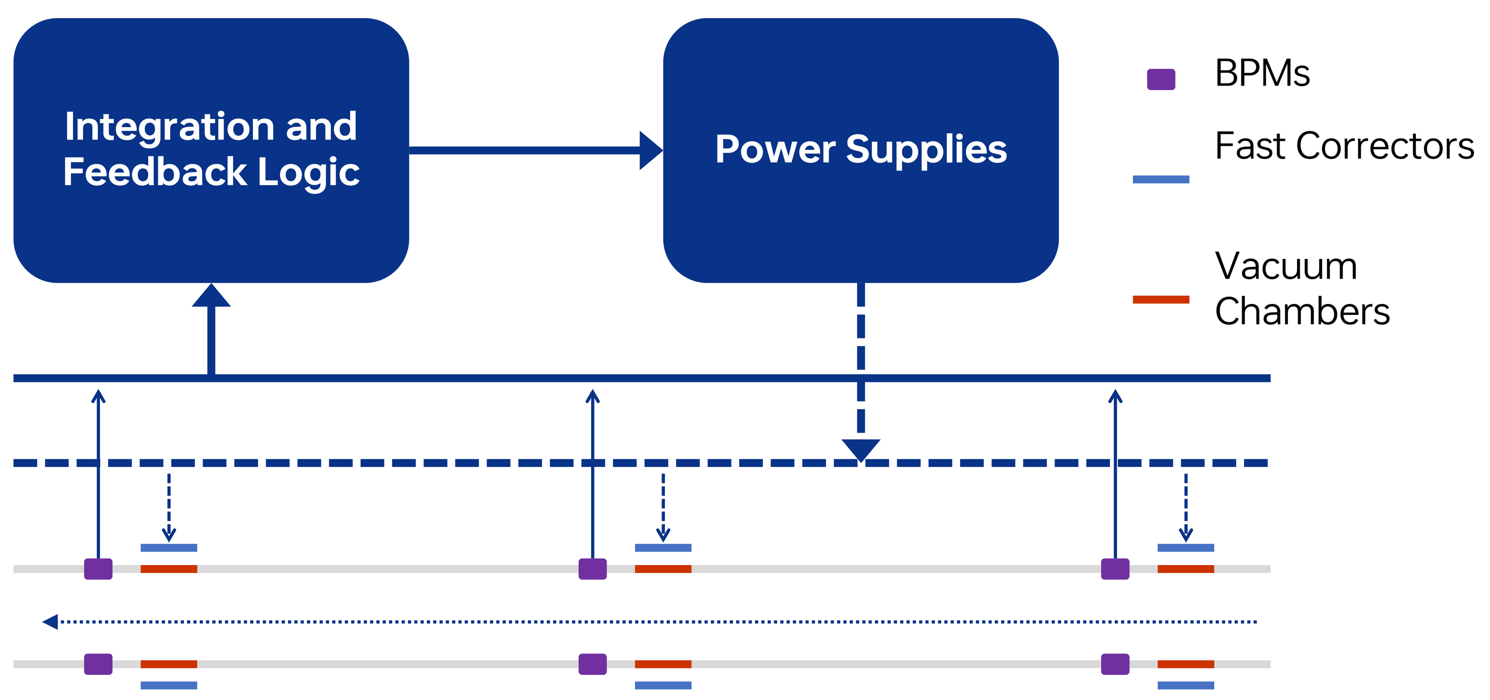

Figure 3 Feedback logic of FOFB

Key Subsystems

Timing system

The timing system is event-based and incorporates both MRF and SINAP MicroTCA bus event system products.

Fast Orbit Feedback System

The SILF storage ring is comprised of 28 cells, with each cell featuring a “cell controller” that forms the foundation of the fast orbit feedback system infrastructure. The implementation of the fast orbit feedback system aims to mitigate various disturbances and enhance orbit stability. The feedback logic of Fast Orbit Feedback (FOFB) is shown in Figure 3.

Machine Protection System

Machine protection plays a crucial role in ensuring the operational availability needed for photon production by implementing dedicated protection functions to prevent component damage.

The machine protection system (MPS) comprises two parts: one is the PLC-based slow protection system (SMPS), and the other is the FPGA-based active interlock system (AIS), which has been implemented to safeguard insertion devices (IDs) and vacuum chambers from the potential thermal damage caused by high-density synchrotron radiation power. Figure 4 shows the layout of AIS architecture and the connection between sub-stations.

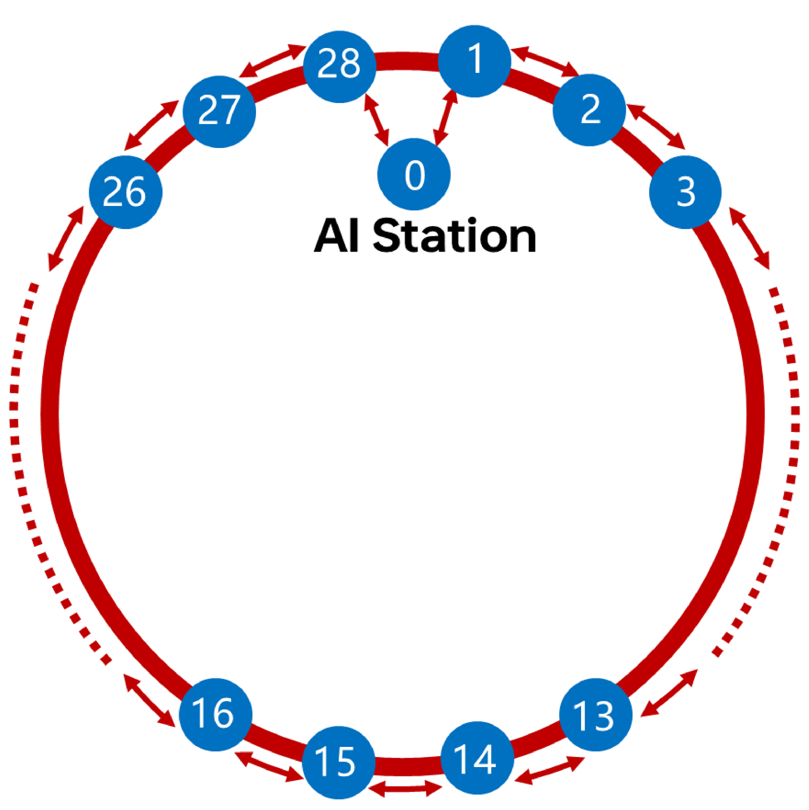

Figure 4 Layout of AIS architecture

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