Integration of an MPSoC-based Acquisition System into the CERN Control System

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Abstract

Future generations of Beam Instrumentation systems will be based on Multiprocessor System on Chip (MPSoC) technology. This new architecture will allow enhanced exploitation of instrumentation signals from CERN's accelerator complex and has thus been chosen as the next platform for several emerging systems.
One of these systems, for the HL-LHC BPM (High-Luminosity LHC Beam Position Monitors), is currently at a prototyping stage, and it is planned to test this prototype with signals from real monitors in CERN's accelerators during 2023. In order to facilitate the analysis of the prototype's performance, a strategy to integrate the setting, control and data acquisition within CERN's accelerator control system has been developed. This paper describes the exploration of various options and eventual choices to achieve a functional system, covering all aspects from data acquisition from the gateware, through to eventual logging on the accelerator logging database. It also describes how the experiences of integrating this prototype will influence future common strategies within the accelerator sector, highlighting how specific problems were addressed, and quantifying the performance we can eventually expect in the final MPSoC-based system

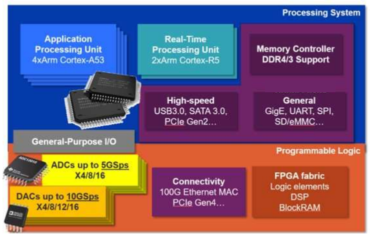
System on Chip

Based on the development board ZCU208 - Xilinx Zynq UltraScale+ RFSoC Gen3

RFSoC is a System-on-Chip integrating a processing system, with programmable logic and high-resolution fast analog to digital converters and digital to analog converters

RFSoC identified as technology for the Hi-Lumi LHC Beam Position Monitor

Xilinx Zynq UltraScale+ RFSoC


Processing System
Application Processing Unit 4xArm Cortex-A53
Real-Time Processing Unit 2xArm Cortex-R5
Memory Controller DDR4/3 Support
High-speed USB3.0, SATA 3.0, PCIe Gen2…
General GigE, UART, SPI, SD/eMMC…
General-Purpose I/O
Programmable Logic
ADCs up to 5GSps X4/8/16
DACs up to 10GSps X4/8/12/16
Connectivity 100G Ethernet MAC PCIe Gen4…
FPGA fabric Logic elements DSP BlockRAM

Xilinx Zynq UltraScale+ RFSoC Box Diagram

System Overview

Analog signals from BPMs connected to RFSoC ADCs

Processing Logic:
•Signal processing and acquisition logic

Processing System
•**Petalinux** OS prepared and deployed on the Application Processing Unit
•**IPBus** based System Configuration Application developed.
•**TCP** Acquisition data transfer application developed.

Front-End Computer
•**FESA** Class for settings & acquisition -> integration in the CERN Control System

NFS & NXCALS
- Settings, acquisition and meta data are logged

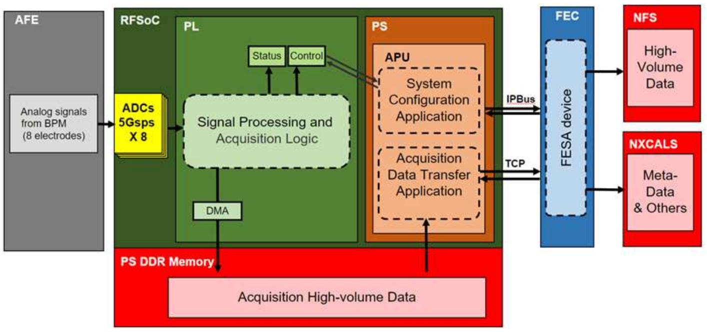
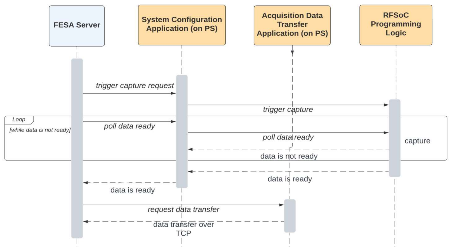

AFE
Analog signals from BPM (8 electrodes)
RFSoC
PL
ADCs 5Gsps X 8
Status
Control
Signal Processing and Acquisition Logic
DMA
PS
APU
System Configuration Application
Acquisition Data Transfer Application
IPBus
TCP
PS DDR Memory
Acquisition High-volume Data
FEC
FESA device
NFS
High-Volume Data
NXCALS
Meta-Data & Others

Diagram of the System

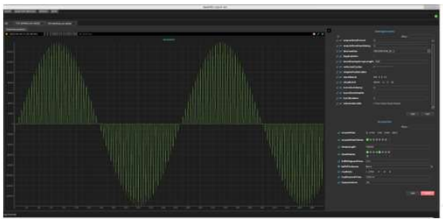
Data Transfer & System Configuration

FESA Server interacts with both system configuration application and acquisition transfer application for:
- Triggering the acquisition
- Polling the status
- Transferring the acquisition data



Sequence diagram of the FESA and SoC communication

GUI



Waveform from the lab test setup displayed in the GUI

PyQt GUI for interaction with the system.

- Depends on PyQt, **pyqtgraph**, generic expert-gui-core library
- Uses the Accelerating Python(**acc-py**) tools and packages.

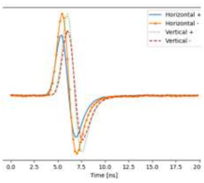
Prototype Validation with Beam Data

RFSoC Installation

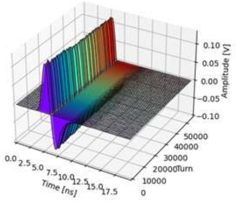
Due to the unavailability for testing purposes of the LHC BPMs, testing the system with a spare SPS BPM was chosen as an alternative.

RFSoC board was installed in a cavern, close to the beam tunnel, isolated from radiation.

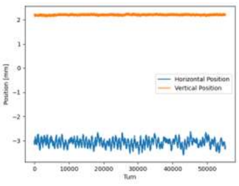
These results match the expected behaviour of the system and have helped us validate the full acquisition, processing and storing chain.



The waveform acquired from 4 different electrodes



Multiple waveforms acquired turn after turn, from a single electrode at each passage of an SPS bunch. Only one waveform every 1000 turns is plotted.



The horizontal and vertical positions in mm as they evolve turn after turn, of the same bunch, computed offline

Conclusion and Outlook

This prototype showcases that SoCs offer a variety of components to leverage. While this poses advantages during the development processes of different systems, it also highlights the need for standardisation of the technical choices.
The experience gained from developing this system provided us with valuable insights into areas that could benefit from improvement:
- The preparation of the operating system image
- Running FESA Servers on the SoC to eliminate the need for a communication layer
- If supporting FESA on SoC is not possible, identification of a standardized communication protocol between a SoC and a FEC

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