



LCLS-II Controls Software Architecture for the Wire Scan Diagnostics

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ABSTRACT

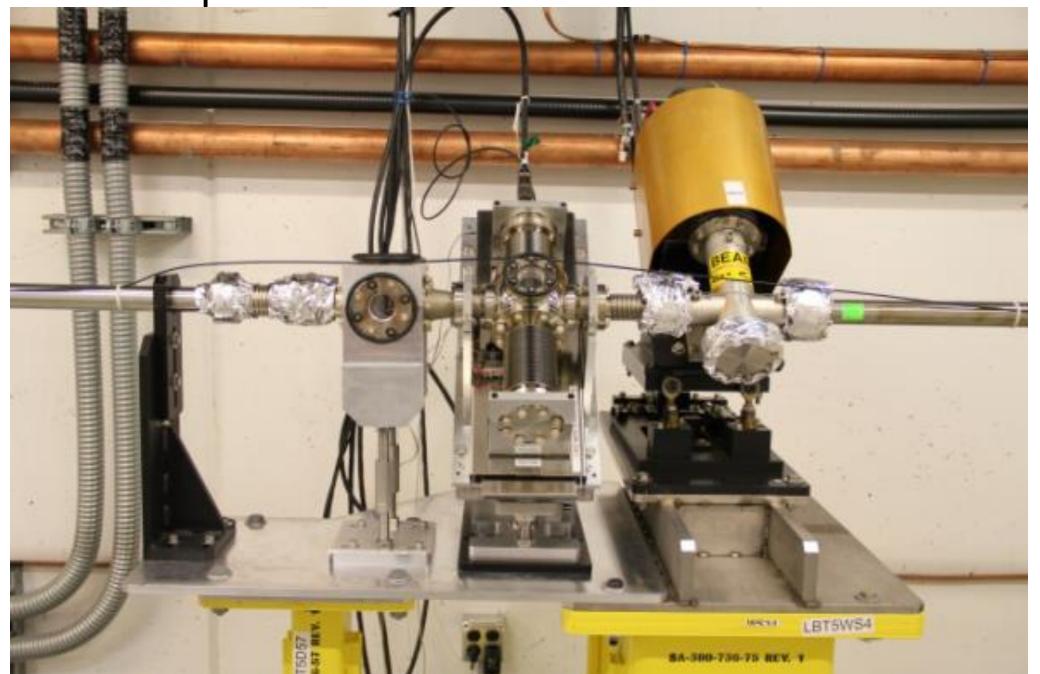
The Super Conducting (SC) Linac Coherent Light Source II (LCLS-II) facility at SLAC is capable of delivering an electron beam at a fast rate of up to 1MHz. The high-rate necessitates the processing algorithms and data exchanges with other similar systems to be implemented with FPGA technology. For LCLS-II, SLAC has deployed a common platform solution (hardware, firmware, software) which is used by timing, machine protection and diagnostics systems. The wire scanner diagnostic system uses this solution to acquire beam synchronous time-stamped readings, of wire scanner position and beam loss during the scan, for each individual bunch. This paper explores the software architecture and control system integration for LCLS-II wire scanners using the common platform solution.

MPS INTEGRATION LOGIC

To prevent damage of wire from higher bunch repetition rates of LCLS-II, wire scanner system has a tie into Machine Protection System (MPS) Logic. For this, a wire scanner must reach a minimum speed before intercepting the beam. The wire scanner must signal the MPS at least 100 us before the wire reaches the beam if the minimum speed has not been reached so that the MPS has time to take preventative action.

DETECTOR DATA DIGITAL INTEGRATION LOGIC

For detection of loss from wire passing through the beam, wire scanner system utilizes the diagnostic output from Beam Containment System's Long Beam Loss Monitor (LBLM) chassis. An external amplifier with adjustable gain is added to facilitate visualization of losses from a wire. The fast diagnostic waveform showing the arrival time of a loss pulse at the Photo Multiplier Tube is used for loss detection. Based on a known loss point and the propagation speed, the peak on the diagnostic waveform can define the location of loss along the beam path. [3]



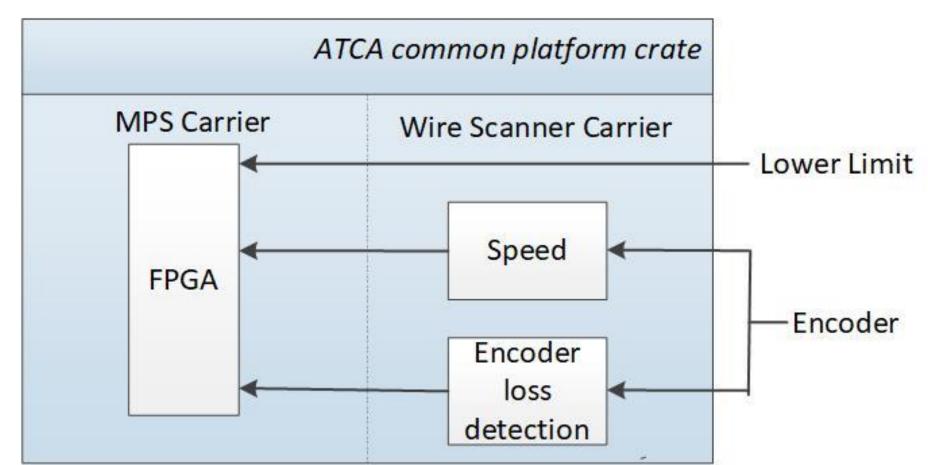
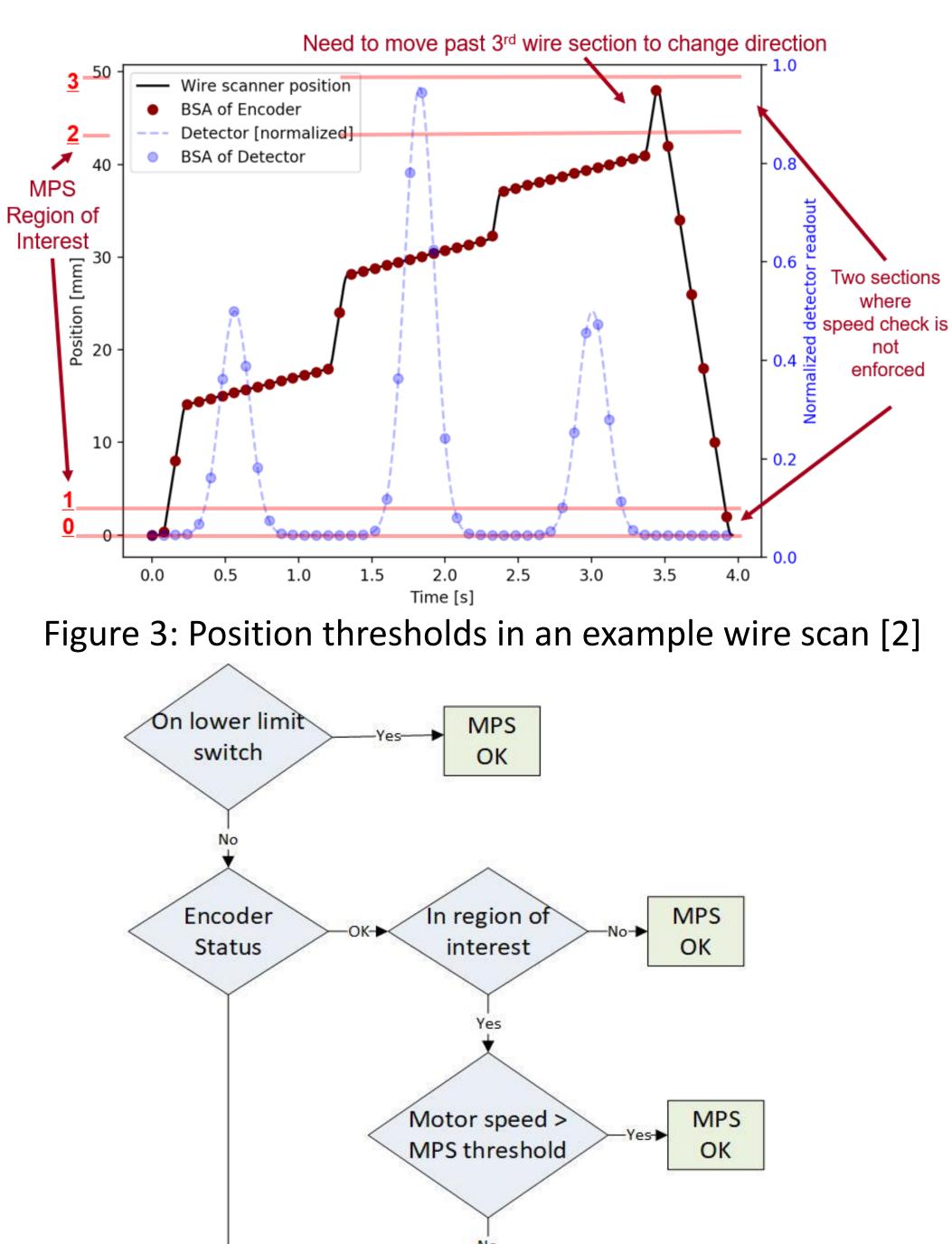


Figure 2: Simple diagram with Inputs to MPS system

MPS fault detection algorithm focuses on 4 position thresholds.

- Lower limit switch position
- Start of region where wire may be present so wire scanner must reach minimum speed.
- End of region of where wire may be present.
- Position where wire scanner will come to a stop to change direction to retract to home/ lower limit.



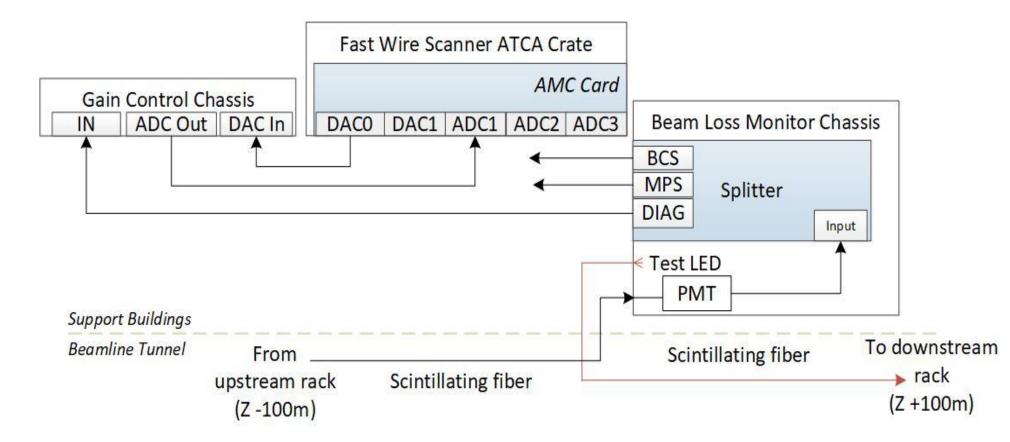


Figure 5: Wire scanner Loss Monitor Schematic

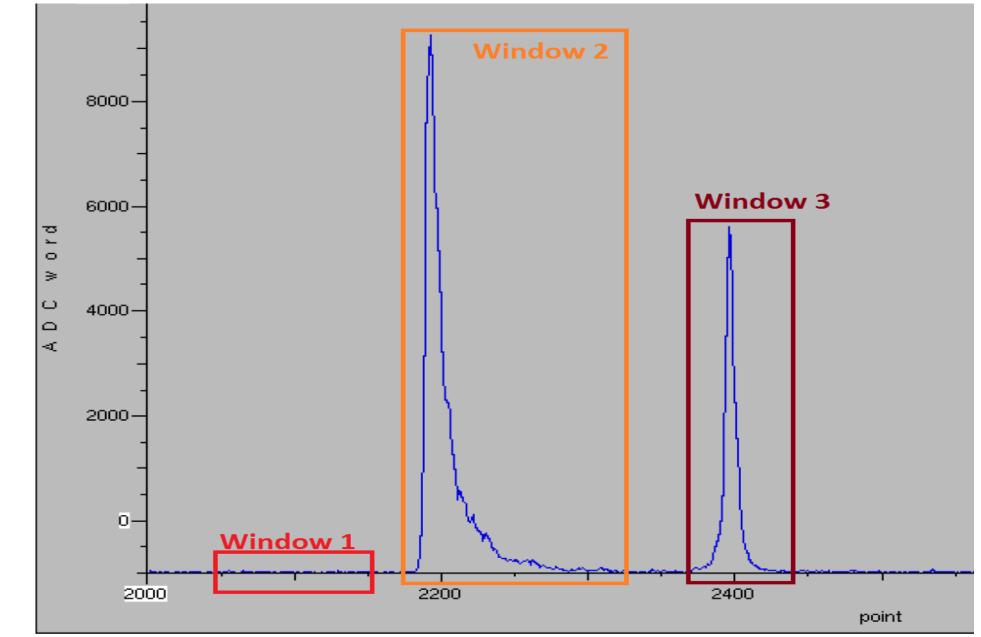


Figure 1: A slow and a fast wire scanner installed in the beamline at LCLS [1]

SOFTWARE STACK

Wire Scanner Controller

Position Feedback Loop s-curve trajectory planning Linear motion profile generation

Axis Fault Handler Task Fault Handler Scope Data collection and transfer

FPGA on ATCA Carrier

Incremental Encoder Position Readback Encoder Fault Detection Motor Speed Calculation Fault Calculation for MPS

Reporting data over diagnostic bus Wirescanner status to Machine Protection System Position and Integrated loss signal to Acquisition Services Figure 6: Example beam loss signal waveform marked with integration windows[4]

Integration algorithm focuses on the windows as shown in the figure.

- Three areas of integration each with its own window start and window width trigger setting.
- The first window selects the pedestal region
- The second window selects the region where beam loss from wire scan may be seen. Also known as gated region.
- The third region is for adjusting non-normalized sums (unused currently).

Result is reported as difference between the gated region and the pedestal region.

.5 × 10 ⁴ LBLM:BPN15:410:A:FAST		corr coef = 0.22	
Y = MX + B	, ,		
M = 0.061		*	
3	*		
	*	*	

EPICS IOC

Desired Scan Velocity Calculation MPS Velocity Calculation Facility Mode Setup Beam Loss Signal Integration Settings for FPGA Trigger settings for Data Acquisition on FPGA

Client Software (User Interface / High Level Applications)

Provide Beam Parameters to controller and ATCA Gaussian curve fitting of measurement points Emittance measurement calculations

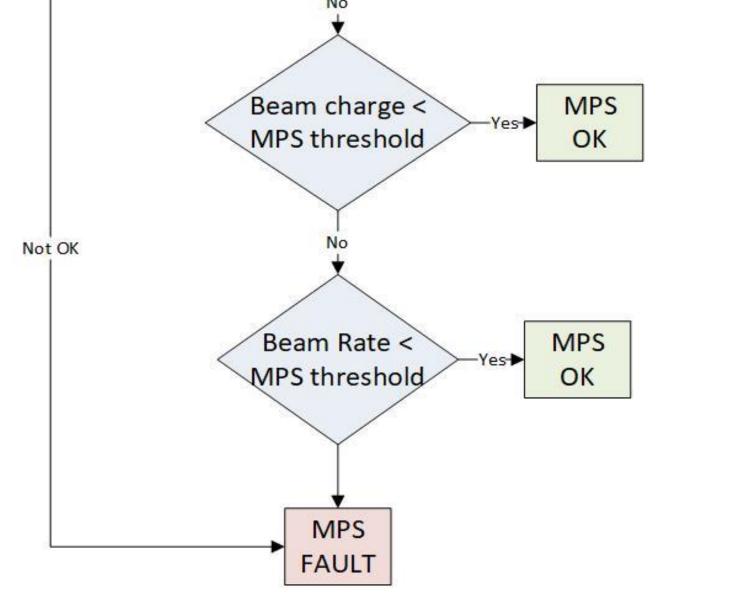
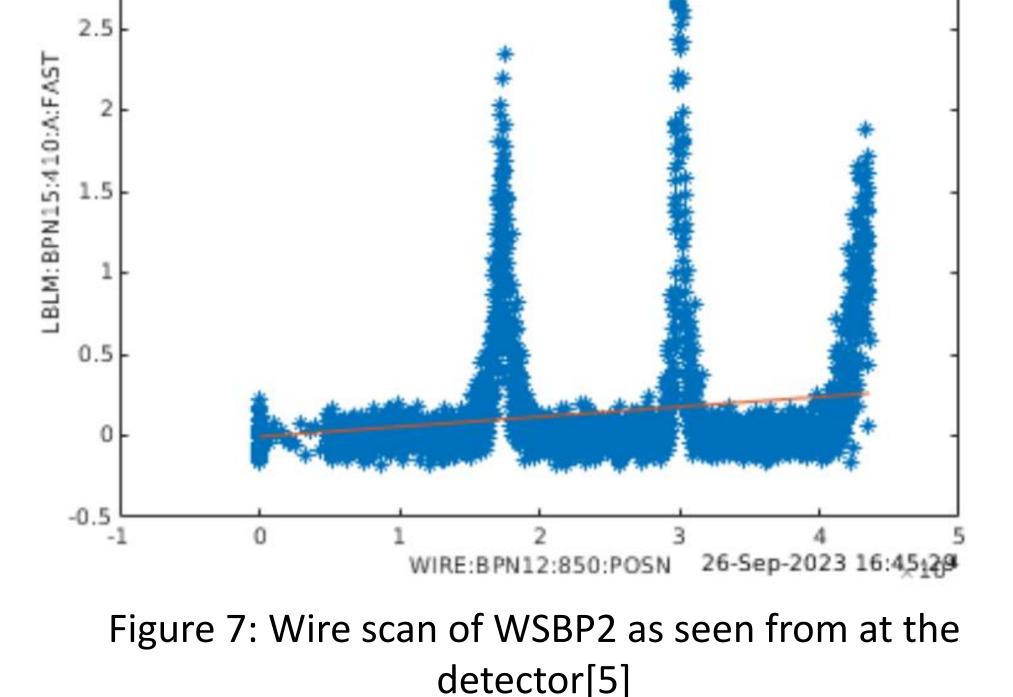


Figure 4: Flow chart depicting Wire Scanner MPS Logic for LCLS-II



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