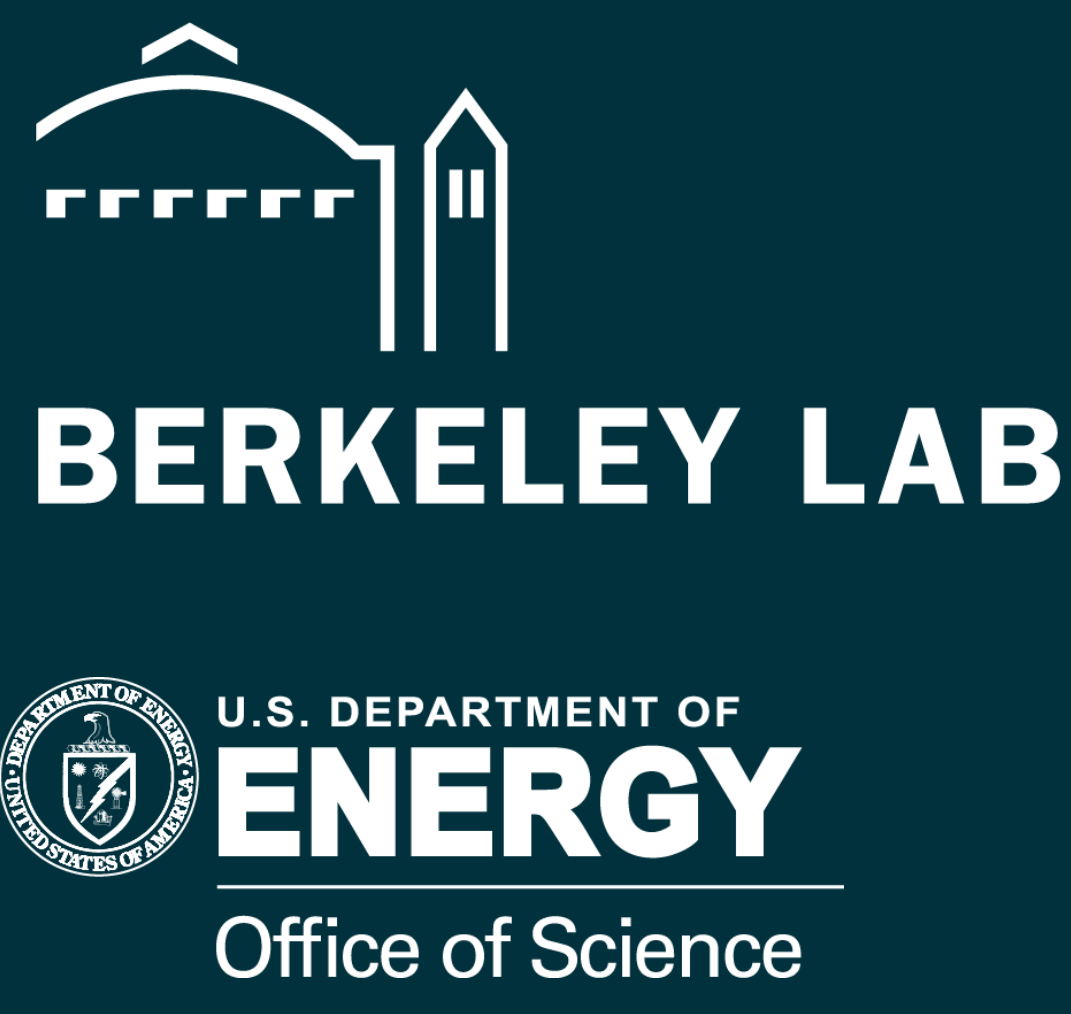


Gateway and Software for ALS-U Instrumentation

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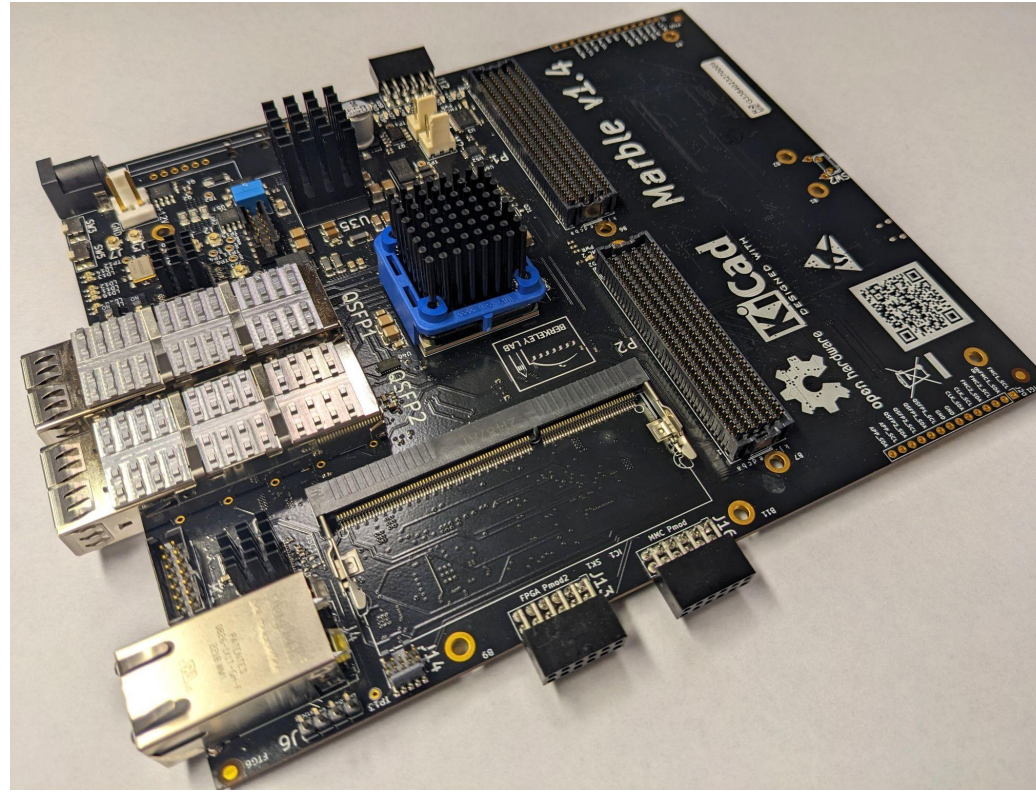


Introduction

The Advanced Light Source Upgrade (ALS-U) is a diffraction-limited light source upgrade under development at the Lawrence Berkeley National Laboratory. The Instrumentation team is responsible for developing hardware, gateway, embedded software and control system integration for diagnostics projects, including Beam Position Monitor (BPM), Fast Orbit Feedback (FOFB), High Speed Digitizer (HSD), Beam Current Monitor (BCM), as well as Fast Machine Protection System (FMPS) and Timing. This work describes the gateway and software approach to these projects, its challenges, tests and integration plans for the novel accumulation and storage rings and transfer lines.

Hardware

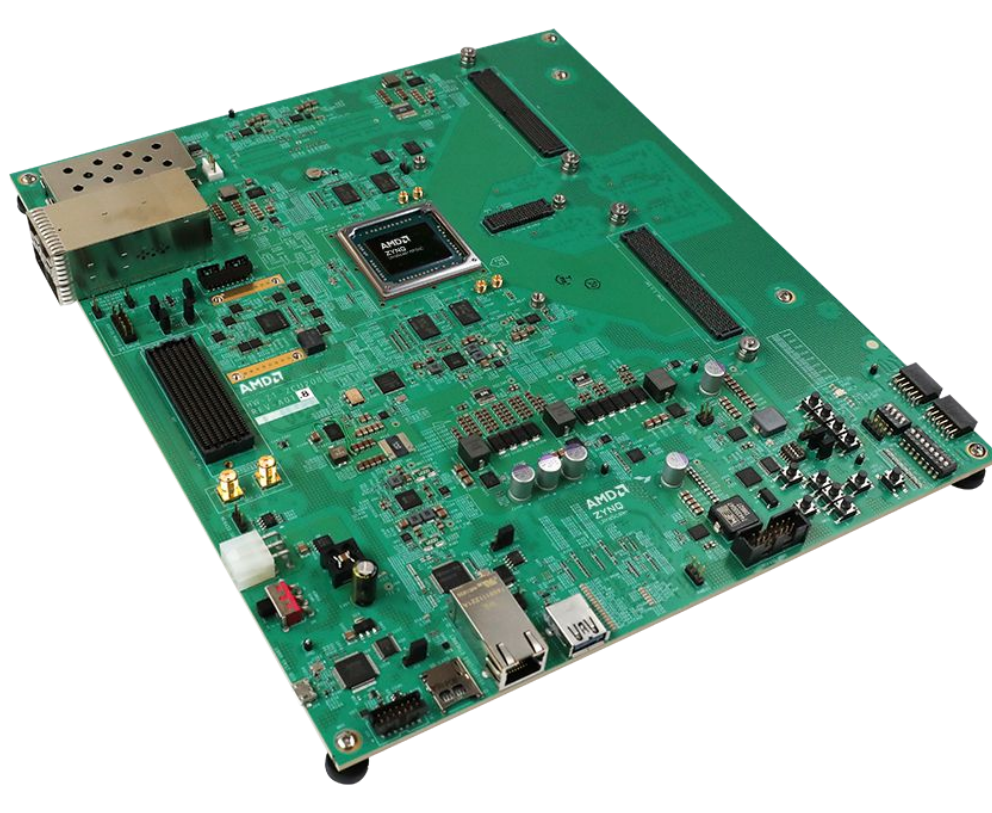
Kintex7 Marble



<https://github.com/berkeleylab/Marble>

RFSoc ZCU111

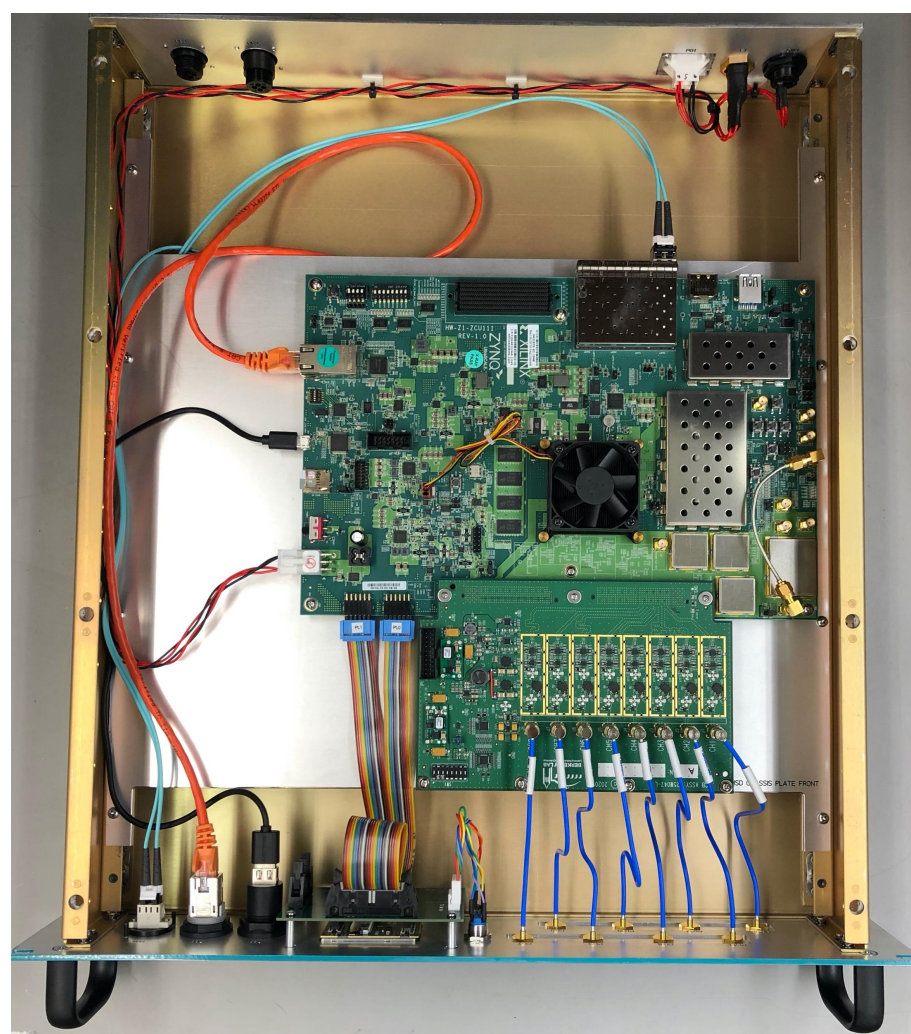
RFSoc ZCU208



<https://www.xilinx.com/products/boards-and-kits/zcu111.html>

<https://www.xilinx.com/products/boards-and-kits/zcu208.html>

High Speed Digitizer (HSD/BCM)



HSD/BCM chassis, 4GSPS, 14-bit ADC (Xilinx ZCU111 platform)

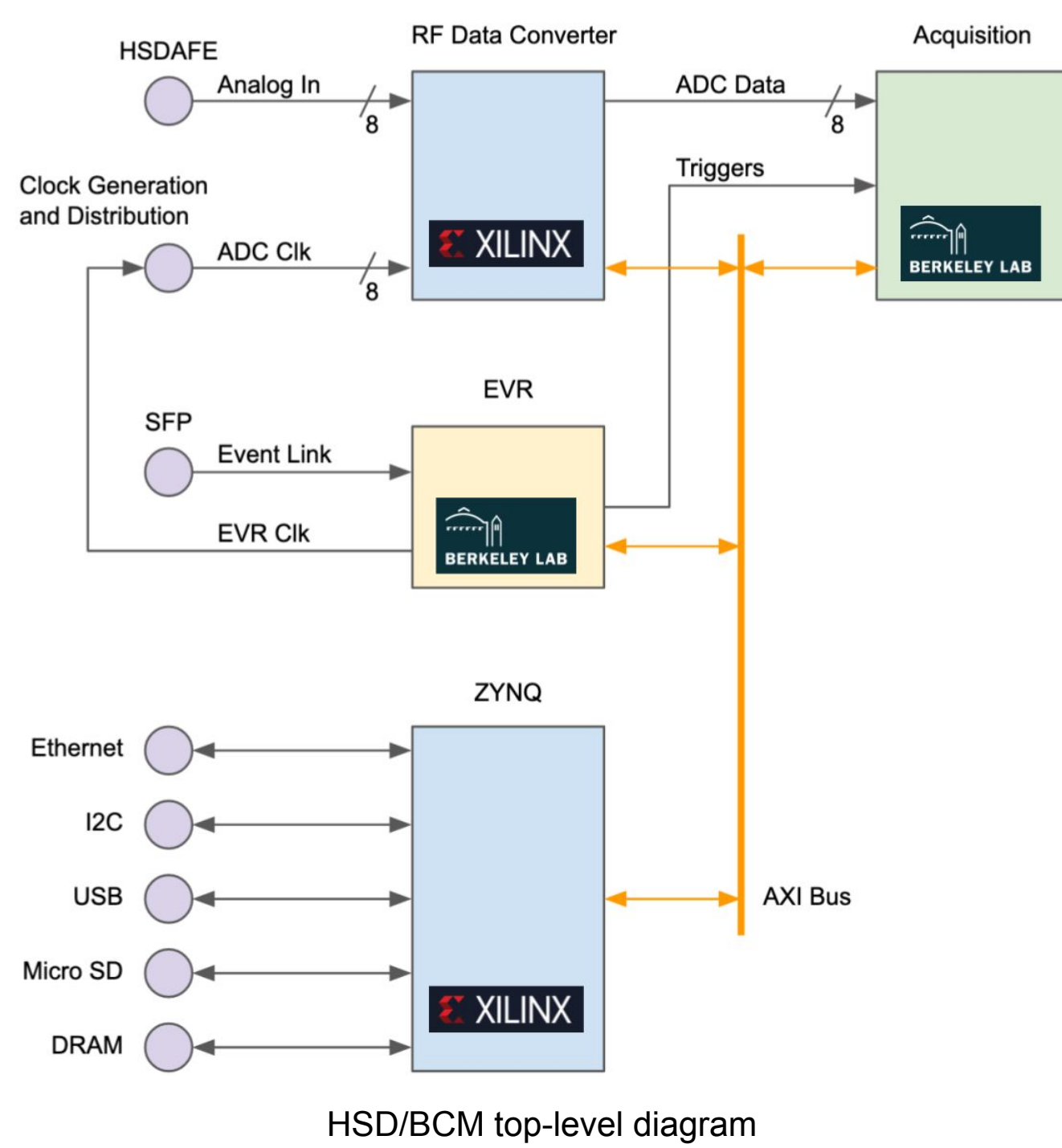
HSD uses a ZCU111 demoboard + an in-house developed AFE to acquire signals at 4GSPS, 14-bit, DC. Timing system synchronized:

- ADC sampling clock
- Triggers
- Timestamp

Gateway components:

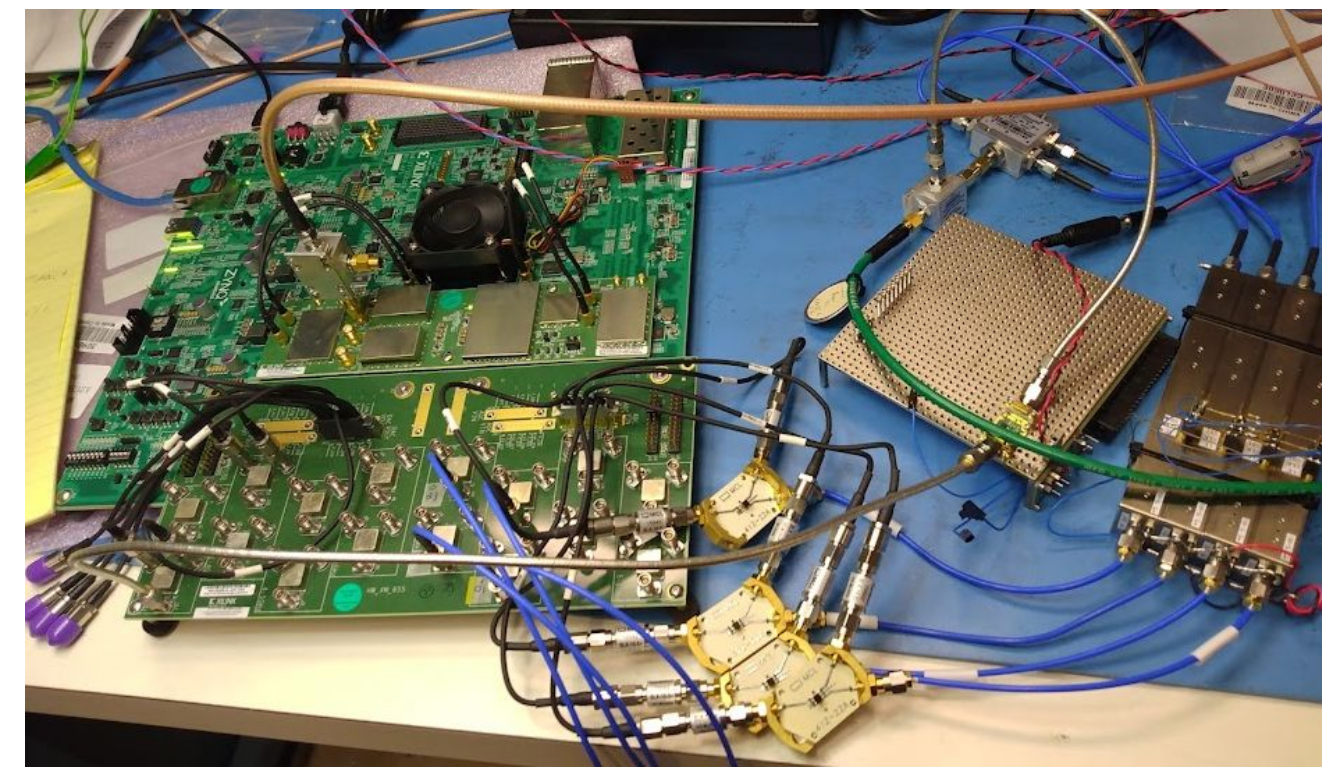
- RFDC module: raw ADC data via AXI-Stream protocol;
- embedded EVR module: recovers RF/4 clock and events from timing link

- Hard-core ARM core: responsible for housekeeping tasks, board control/status and EPICS interface
- Acquisition module: captures either the raw ADC data directly into BRAM (HSD) or a sum at each point, similar to a sampling oscilloscope (BCM)



HSD/BCM top-level diagram

Beam Position Monitor (BPM)



RFSoc BPM bench setup, 5GSPS, 14-bit ADC (left: Xilinx ZCU208 platform, right: 4 AFE modules)

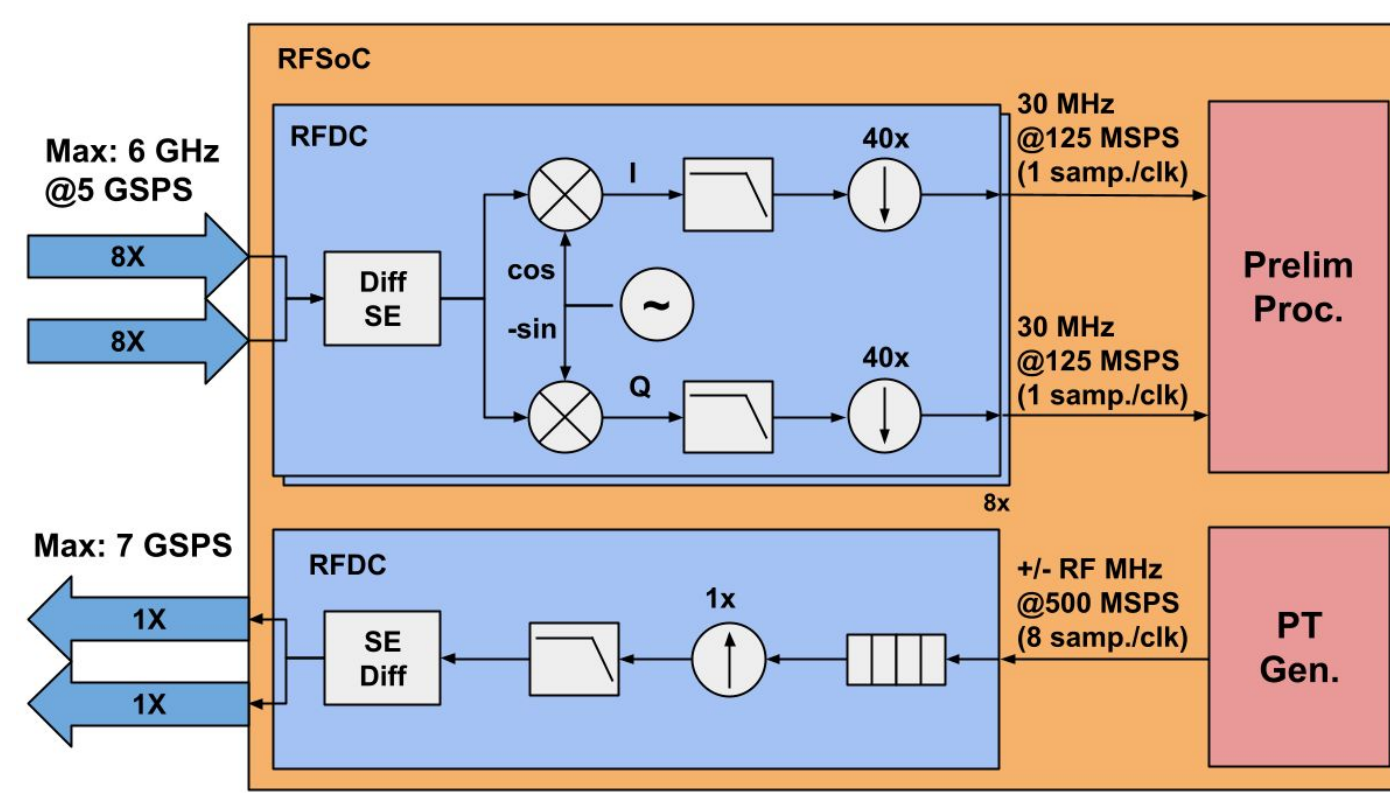
$$ADC_{freq} = \frac{RF * N}{h} * D$$

$$ADC_{freq} = \frac{500 * 81}{328} * 40$$

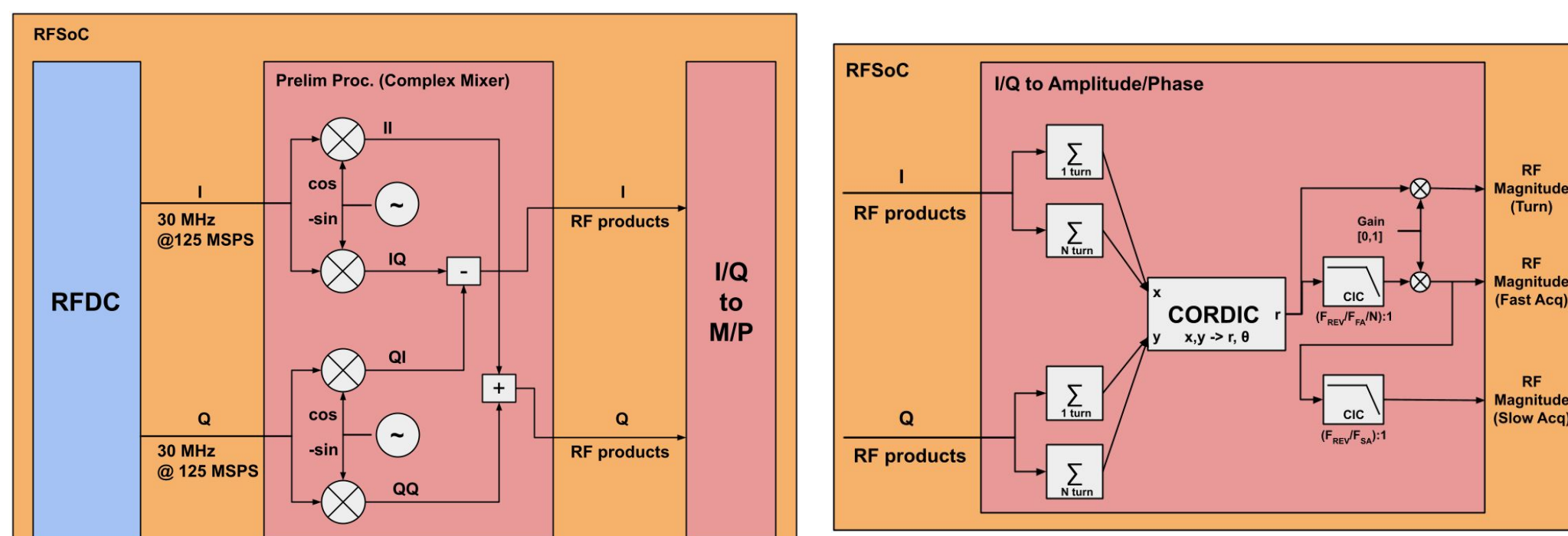
$$ADC_{freq} = 4,939 \text{ GSPS}$$

BPM 500MHz AFE channel

Open source gateway and embedded software consisting of: 2-stage DDC for amplitude demodulation; flexible acquisition engine to external SDRAM, continuous pilot tone calibration, rich status monitoring.



RFSoc BPM first DDC stage and PT generation

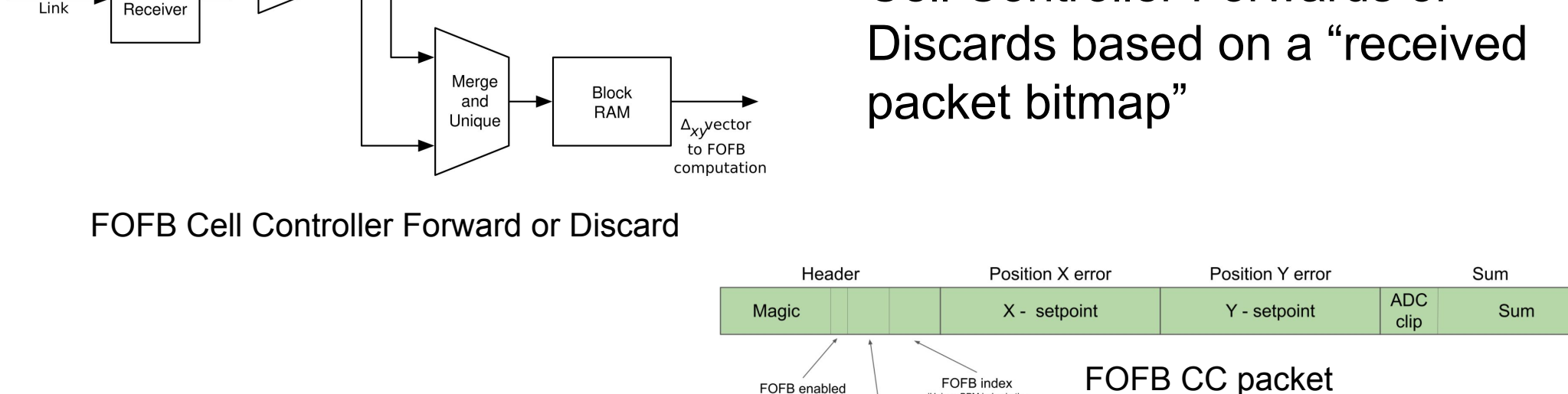
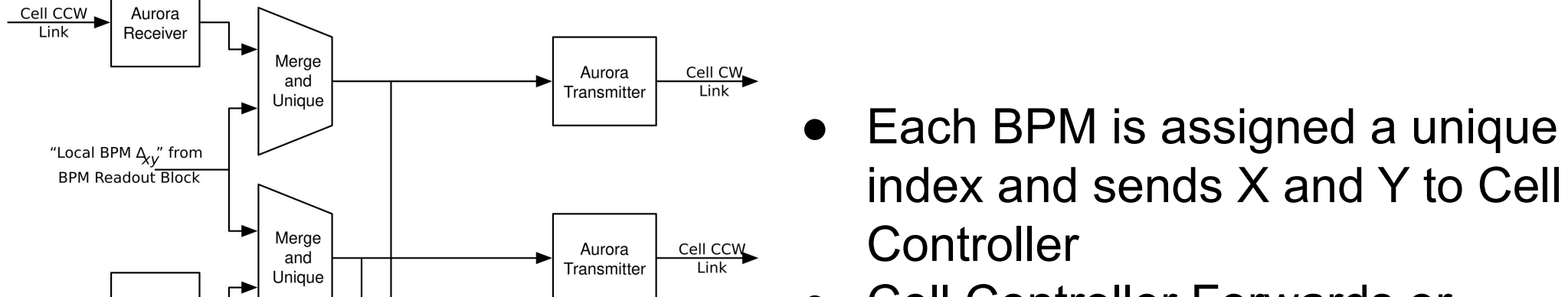
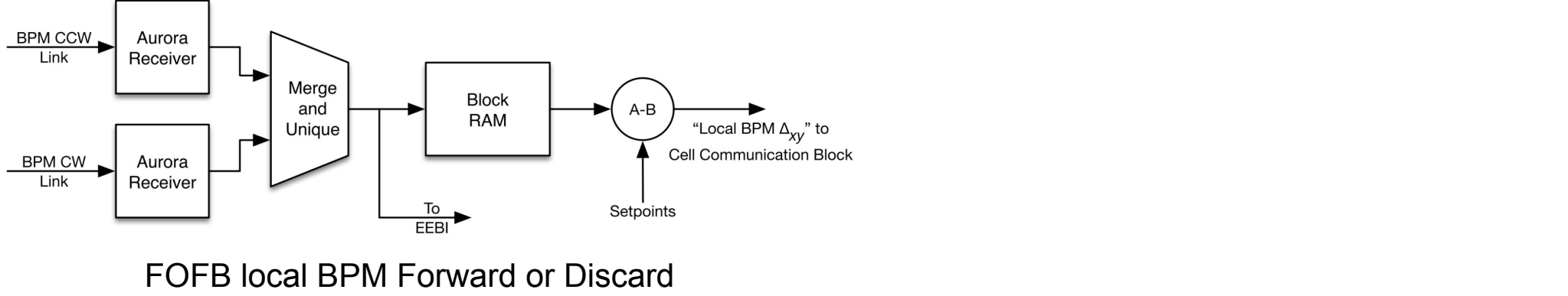
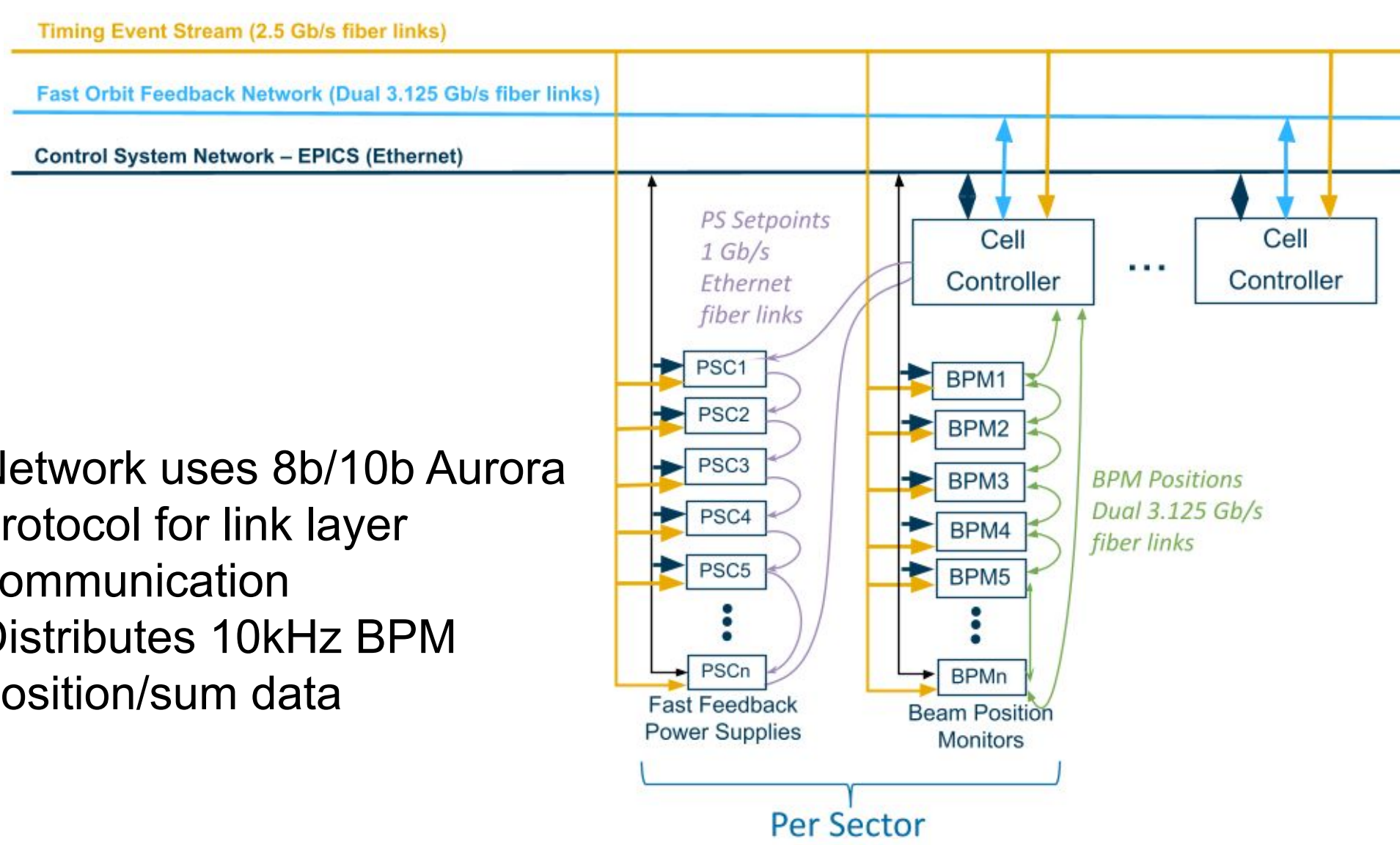


RFSoc BPM second mixer stage

RFSoc I/Q to Amp.Phase + filters

Fast Orbit Feedback (FOFB)

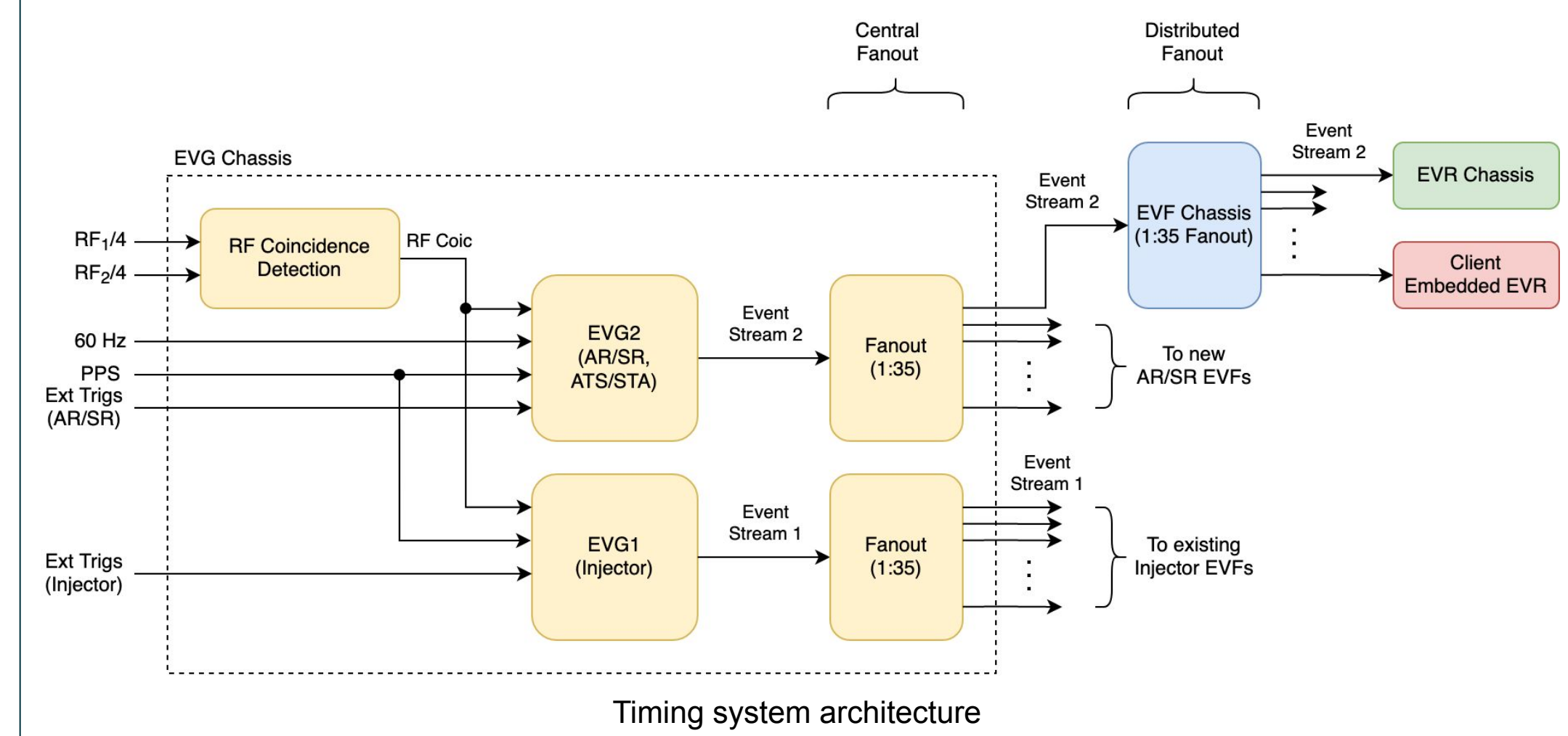
Dual ring topology for BPM to Cell and Cell to Cell data distribution. Single ring, UDP/IP, for PSC setpoints.



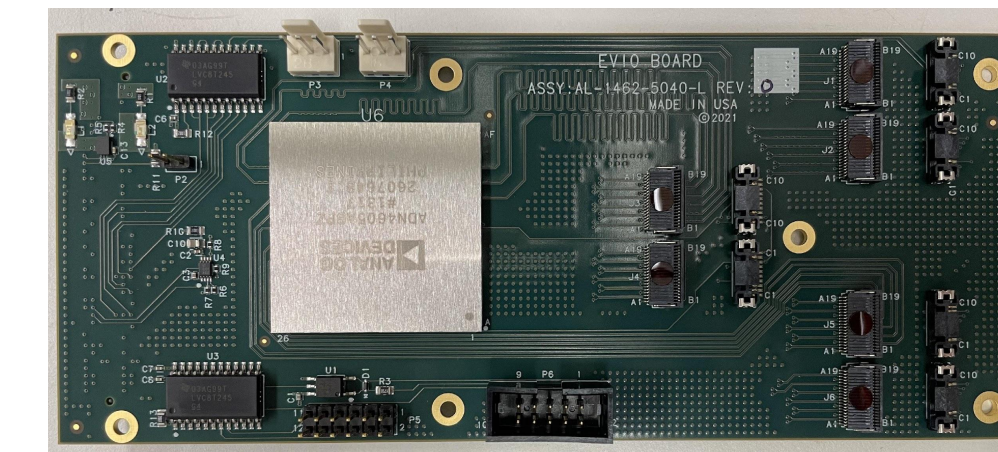
- Network uses 8b/10b Aurora protocol for link layer communication
- Distributes 10kHz BPM position/sum data

- Each BPM is assigned a unique index and sends X and Y to Cell Controller
- Cell Controller Forwards or Discards based on a "received packet bitmap"

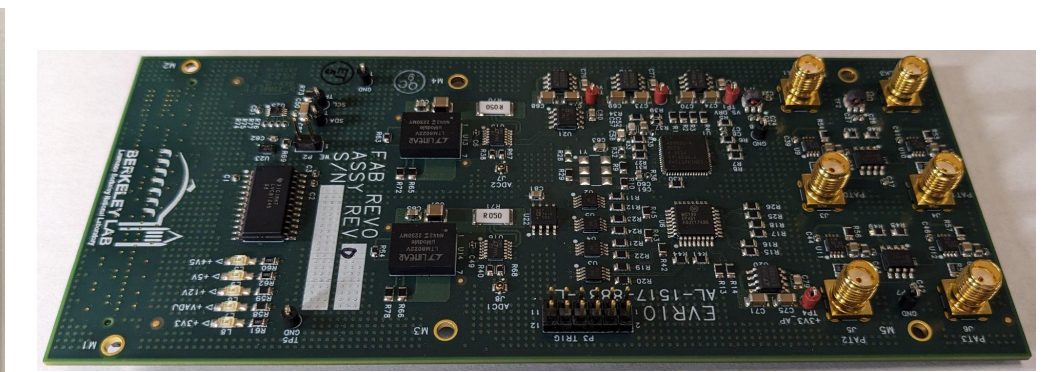
Timing



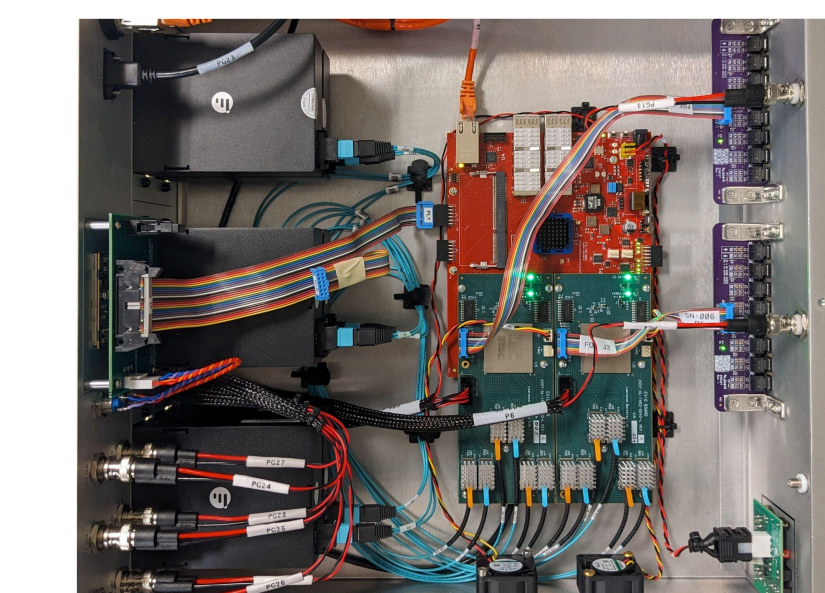
Timing system architecture



FMC EVIO



FMC EVRIO

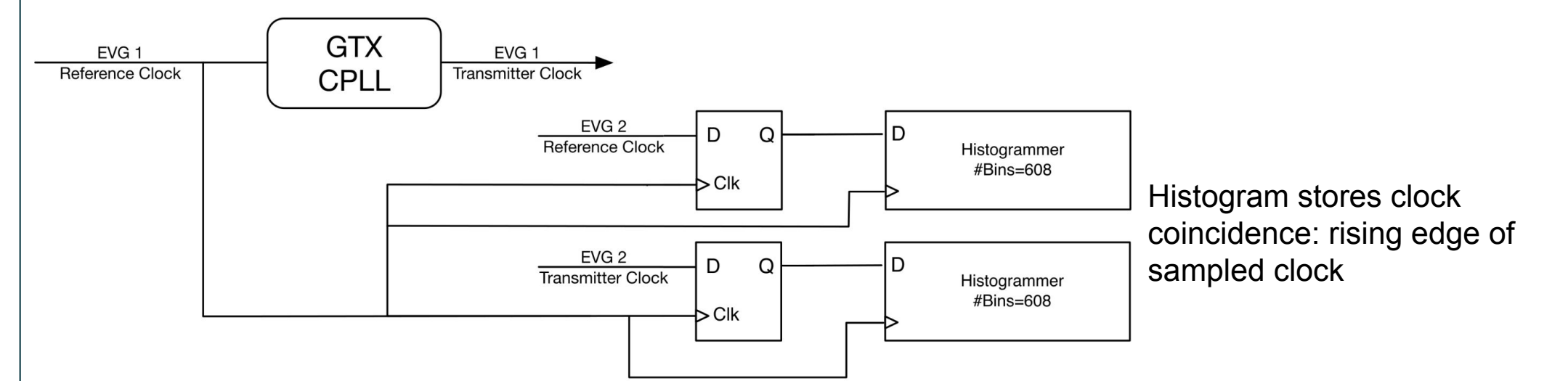


ALS-U Timing EVG

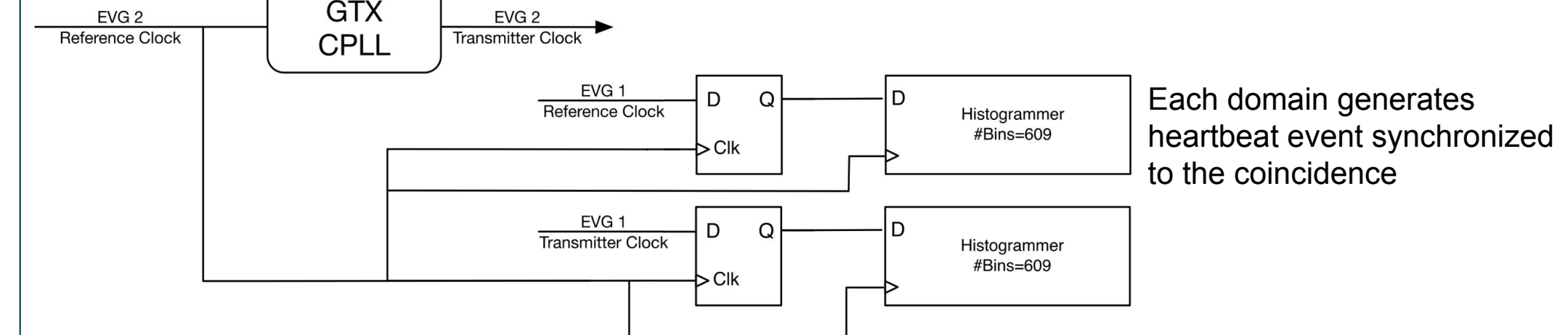


Firefly cable and fiber cassette

ALS-U timing system needs to support injection across 2 different RF domains RF_{inj} and RF_{sr} with $RF_{inj} = 608/609 * RF_{sr}$.



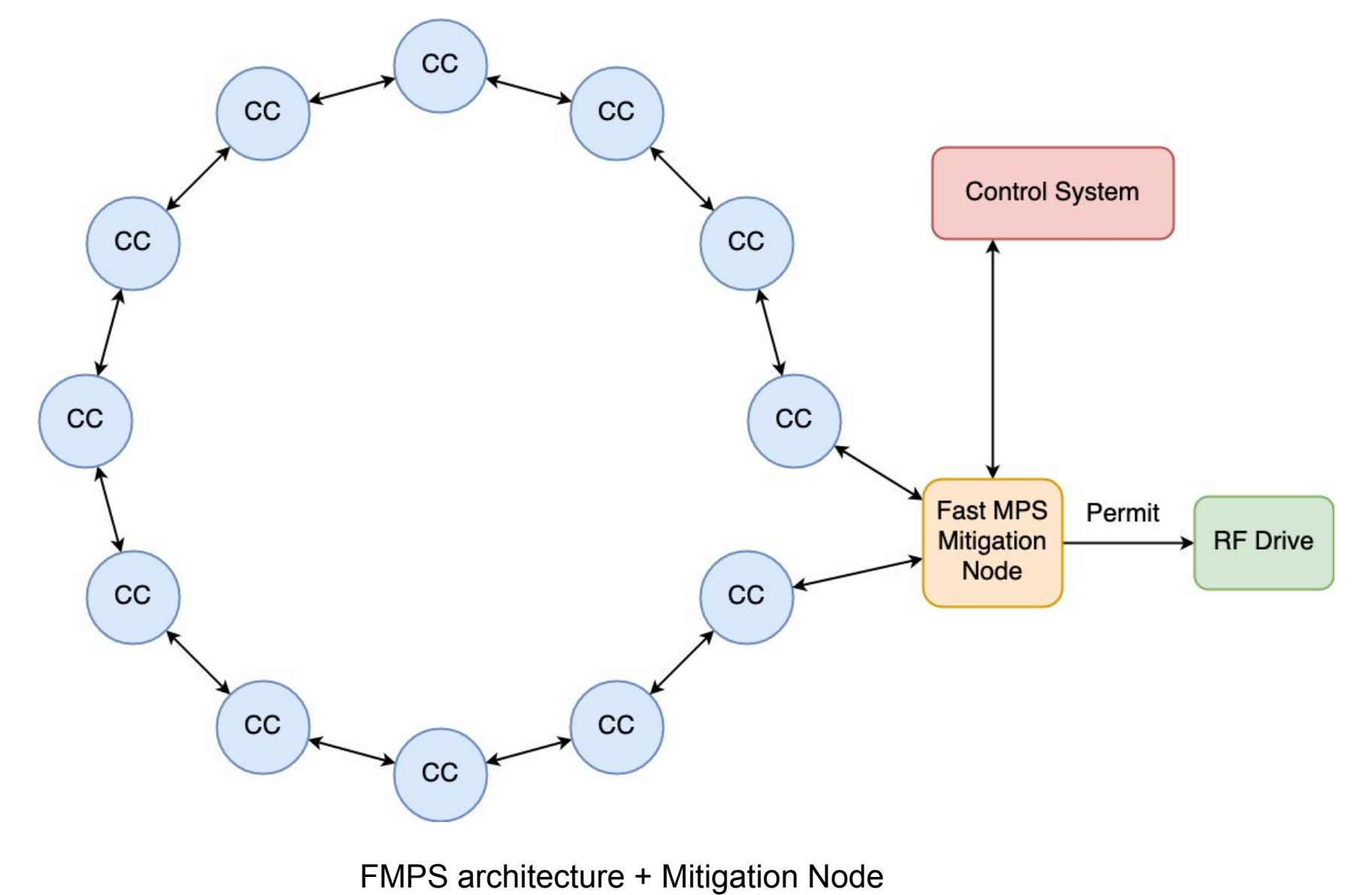
Histogram stores clock coincidence: rising edge of sampled clock



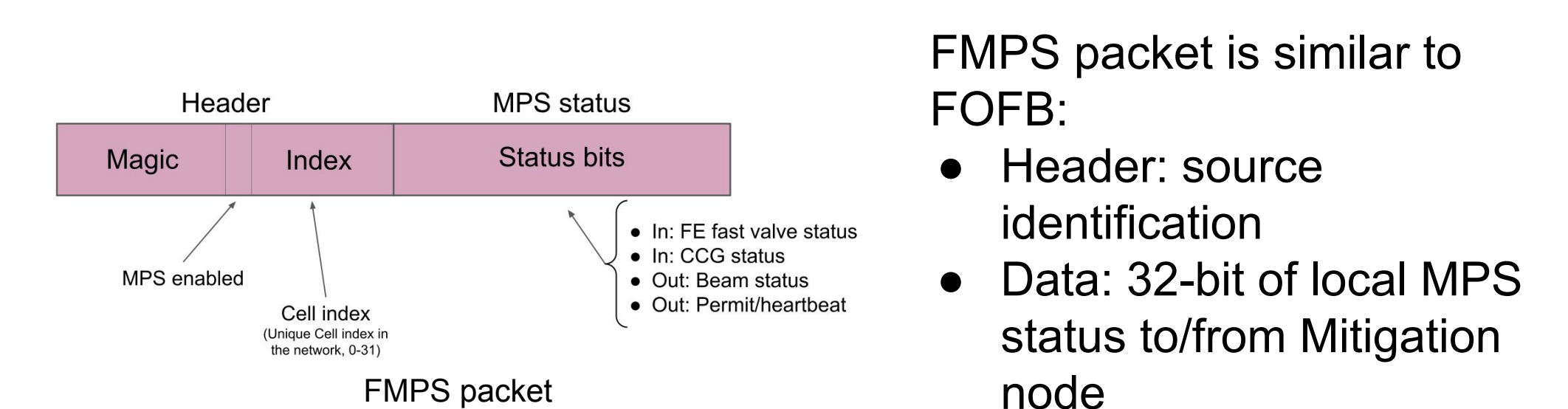
Each domain generates heartbeat event synchronized to the coincidence

Fast Machine Protection System (FMPS)

FMPS shares the FOFB deterministic network and uses the Cell Controller nodes to inject new FMPS packets into the network. Mitigation node acts like a 13th node and uses position data + status to act on RF.



FMPS architecture + Mitigation Node



FMPS packet is similar to FOFB:

- Header: source identification
- Data: 32-bit of local MPS status to/from Mitigation node