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Application Development on CPCI-S.0 Hardware at PSI

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Abstract

A Hardware and Software Toolbox is being created to accelerate the engineering of electronic components for large facility upgrades at the Paul Scherrer Institute. This Toolbox consists of modular hardware that follows the CPCI-S.0 concept and base designs. The goal is to provide a starting foundation, tools, modules and libraries to simplify and accelerate developments. Base designs provide advanced starting points for applications on AMD Zynq™ Ultrascale+ devices. They are an environment of basic ready-to-use system and functional building blocks organized into two main layers: one for the Processing System (PS) and one for the Programmable Logic (PL). The former is a collection of the software packages that run within an Operating System. The latter, lower layer consists of a seed Vivado project, library of firmware components and ready-to-use modules. Furthermore, a set of device-tree-overlay scripts simplifies the creation of high-level connections between the two layers.

Keywords: CPCI-S.0, MPSoC, AMD Zynq UltraScale+, Toolbox

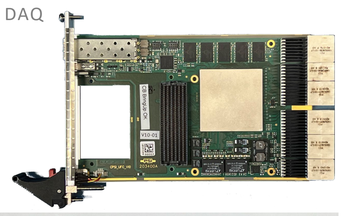
CPCI-S Hardware

CPCI Crate:

- 9 front slots (1 system, 8 peripheral)
- plus rear, utility, SysMon and 3xPower Supply
- Full Mesh of Multigigabit connections (P6)
- PCIe, USB (2.0 and 3.0), SATA and/or Multigigabit (system slot star topology)
- I2C backplane bus

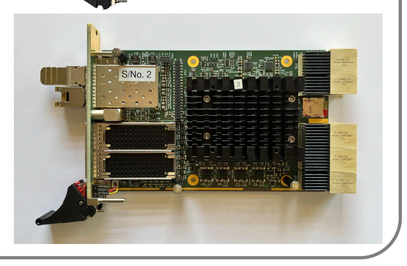
Custom Cards:

- CPSI_UFC, Universal FMC-Carrier when loaded with a FMC DAC/ADC it becomes a complete DAQ
- CPSI_CIO, Communication IO card for Serial IO with two SFP+ and two QSFP+
- CPSI_RTM_DAC contains two 16 bit 500Msps DAC, two SFPs and an expansion connector
- CPSI_RTM_FIO io board with one SFP+, two SMA 500MHz and eight LEMO
- CPSI_CM1, a crate control and monitoring card
- Test Cards: Power Load, MGT loopback, etc.



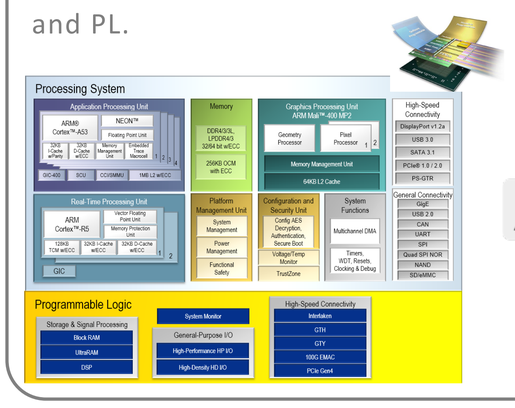
Commercial Cards:

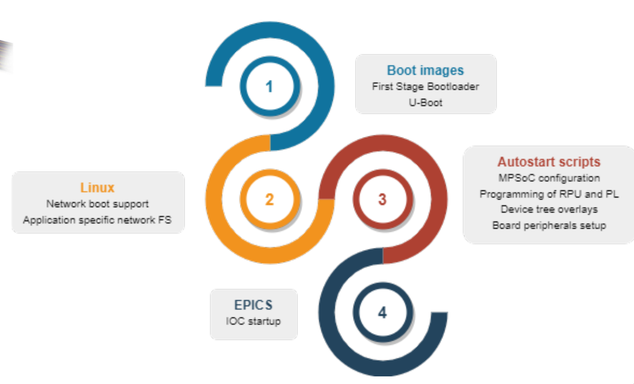
- SC5 Festival (EKF), High Performance CPU Board
- SD1-DISCO (EKF), CPCI-S SATA Drive Carrier Board
- FMC cards, like the ADC3110: COTS FMC module with an 8ch, 250MHz ADC



Multiprocessor System on Chip

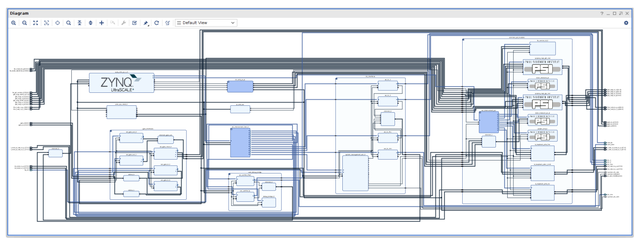
A Zynq™ UltraScale+ MPSoC device is at the center of the main custom FPGA cards (UFC and CIO). MPSoC devices simplify real-time control and data acquisition systems by integrating an array of system components into a single device: Arm Cortex-A53 Application Processing Unit (APU), an Arm Cortex-R5F real-time processing unit (RPU), a Mali-400 graphics processing unit (GPU) and programable logic (PL). Linux, EPICS soft IOCs and custom software run directly on the APU, while the real-time signal processing is offloaded onto the RPU and PL.

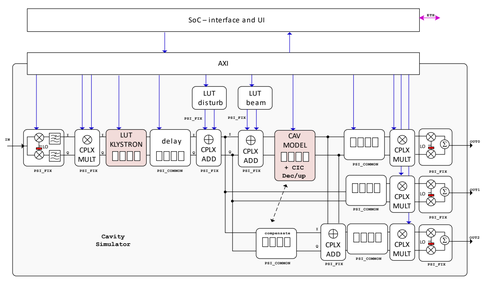




Firmware

A library* of firmware components is available and maintained on GitHub to accelerate the application development in the PL. These components are grouped into signal processing elements and commonly utilized functional blocks. The former library, psi_fix, is an array of fixed point arithmetic entities like: FIR and IIR filters. The latter library, psi_common, contains communication interfaces (axi, i2c, spi, …) and basic data processing elements like FIFOs and clock domain crossing elements. These components are utilized to aid the development of both the application specific tasks and reusable high-level ip-blocks that can be simply instantiated in the block design on the AXI bus like: fw identification, clock measure, mgt testing and adc interfaces. Block and code level examples of library components instantiation are provided below:





*https://github.com/paulscherrerinstitute/psi_fpga_all

Software

Modular software layers glue all levels of the system together and simplify the development and maintenance. Board specific (UFC, CIO, etc.) base designs provide ready-to-use boot images that configure the PS, network boot a common Linux and network mount the application specific filesystem. After booting the OS a collection of reusable bash AutoStart scripts configure the MPSoC processing units (PL and RPU), load device tree overlays, setup on-board peripherals and finally start the EPICS soft IOCs. These scripts are written in a generic, reusable fashion to support application and board specific features. For example, the device tree overlay scripts take the description of the PL instantiated component (like: axi address, numbers, names) to prepare the logical-name binding for the user-space software drivers and tools (like: gpioget, gpioset, i2cget, i2cset). On a higher level, maintained python packages and C libraries facilitate the application development process by providing top-level interfaces to the low level components (axi-communication, shared memory, u-art, drivers for modules in the PL, and peripheral chip configuration). We have also developed a python package to automate testing and report generation.

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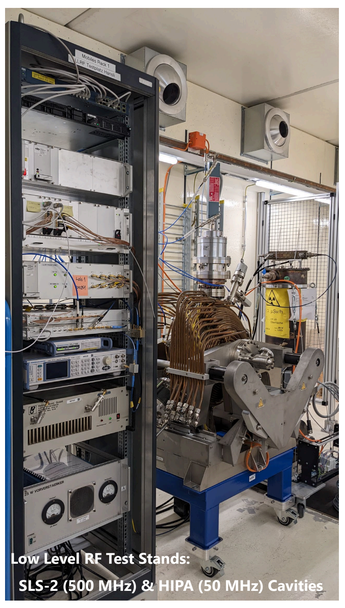
Applications



This new processing platform is versatile and can be uses for several applications around accelerator technologies such as LLM, PCT, ICT, FPM and LLRF systems. This solution allows reusing templates and continuing improving interoperability to satisfy the requirements for each instrumentation. As a generic electronic data acquisition CPSI-UFC and CPSI-CIO, with custom cards or COTS cards (like: FMC), connect fast control and acquisition channels to the machine network.

Conclusion

A CPCI-S.0 toolbox is being constructed to increase the speed and efficiency of application development at the large facilities and accelerators of PSI, like HIPA and SLS 2.0. It is an ecosystem of compatible and ready-to-use components that creates the complete environment for electronics measurement and control systems. Standard interfaces (PCIe, USB, Sata, i2c, multigigabit serial links) on the backplane combined with the state-of-the-art electronics (AMD Zynq™ UltraScale+ MPSoC, custom electronics and COT cards) make the CSPI-S.0 a versatility hardware platform with extreme potential. A common network booted OS, base designs, software packages, firmware libraries and reusable IP modules provide engineers and scientist a quick start and allow them to focus on the specific application. A handful of initial applications have already demonstrated the capabilities and strengths of the toolbox.