The Timing System for PETRA IV.

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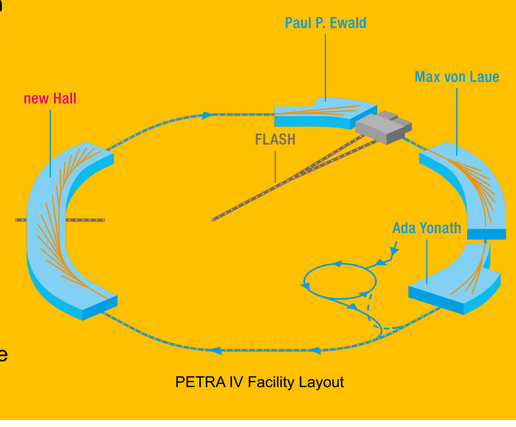
PETRA IV – The Next-Generation Light Source

Upgrade of the existing 2.3 km synchrotron radiation source **PETRA III** into a multi-bend achromat (MBA) based ultra-low emittance storage ring:

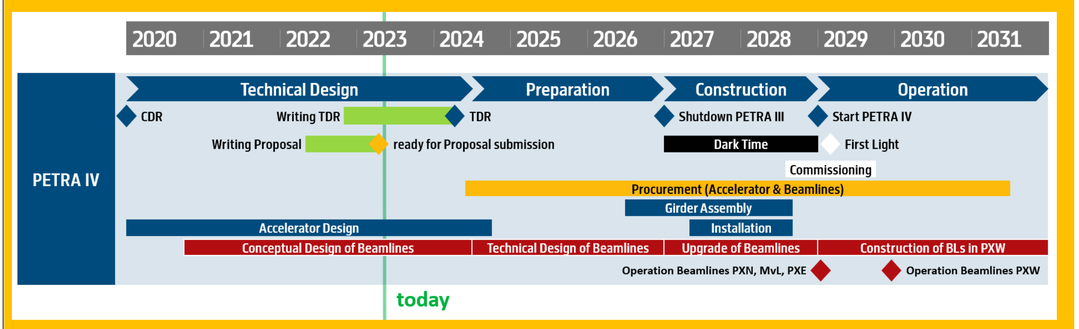
- **6 GeV** electron beams
- **10-30 pm rad** horizontal emittance
- **< 10 pm rad** vertical emittance
- **500 MHz** (499.6643 MHz) RF reference
- **80/1600 bunches** in timing/brightness mode

- New booster synchrotron (DESY IV)
- New experimental hall on the West side
- **30 beamlines** in 4 experimental halls

- Alternative, plasma-based injector substituting the DESY IV booster and LINAC II injector chain



PETRA IV Facility Layout



PETRA IV Roadmap

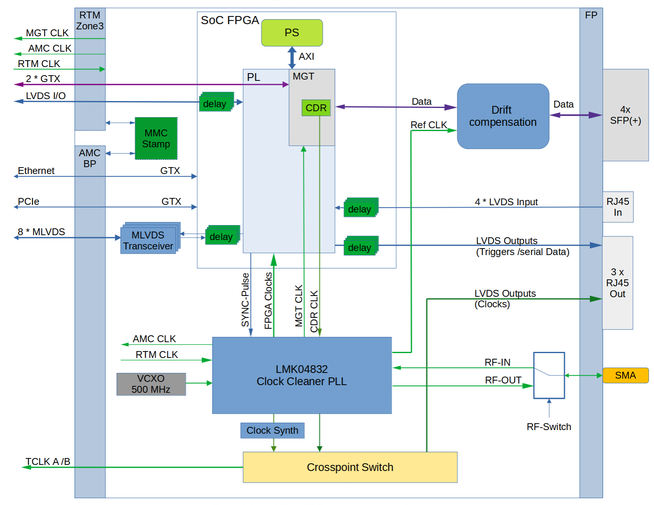
Hardware Development - DAMC-X3TIMER Module

The design of the **DAMC-X3TIMER module** is based on the concept and functionality of the X2TIMER AMC used at European XFEL and FLASH. It is adapted and enhanced to fulfil the requirements of the PETRA IV machine and pre-accelerator chain:

- Assemble a timing event data block (consisting of trigger signals and operation-related data) and transmit it over optical fibre @0.5 Gbps using the 500 MHz RF reference
- Compensate drifts due to environmental effects in transmission/redistribution of the optical stream
- Generate low-jitter clocks for internal and external use from the RF reference received from the master oscillator or recovered from the optical input stream
- Recover the trigger signals and operation-related data from the input stream
- Distribute clocks, triggers and data to local clients through front panels, AMC backplane and RTM connector
- Interface to the local CPU AMC via PCIe for configuration, control and monitoring purposes

4U MTCA.4 double mid-size AMC board holding:

- **1 SoC FPGA** to generate and distribute timing signals and communicate with the host CPU
- **1 Drift compensation logic unit** (on daughter card)
- **1 Dual loop clock cleaner** with 2 PLLs to reduce clock jitter and derive clocks
- **1 Custom tunable VCXO** for clock cleaner PLL
- **1 Clock synthesizer** to generate individual frequencies for distribution
- **1 Crosspoint switch** for clock distribution
- Multiple coarse and fine programmable delay lines
- Various front panel I/O connector types
  - SFP/SFP+ Timing Data Stream Rx/Tx
  - SMA RF Input/Output
  - RJ45 LVDS I/O (Clocks, Trigger, Data)
- Zone 3 to support digital class D1.1 RTM modules



DAMC-X3TIMER Hardware Schematic

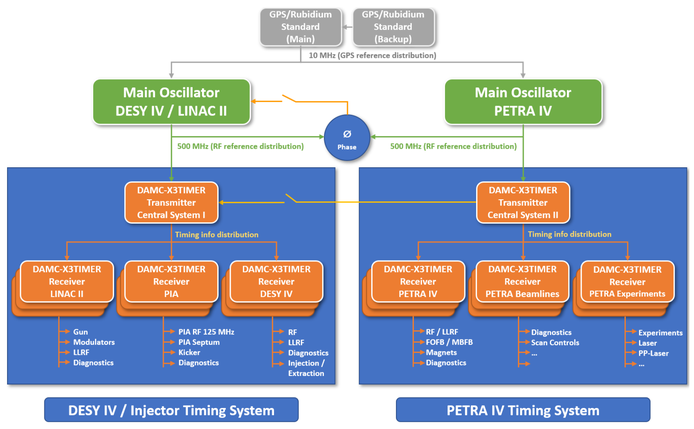
PETRA IV Timing and RF Synchronisation Systems

Completely redesigned to match the **PETRA IV** requirements. Provide synchronisation for operations and processes across the main storage ring, injector chains and experimental beamlines.

RF Synchronisation System

Provides continuous reference RF signals generated by a unique, stable master oscillator to drive local, low-noise oscillators:

- **500 MHz** to PETRA IV & DESY IV fundamental RF systems
- **1.5 GHz** to PETRA IV 3rd harmonic RF system
- **125 MHz** to PIA (bunch compressor) 12th harmonic RF systems
- **3 GHz** for the plasma-based injector source



Exemplary layout of the two systems for the PETRA IV storage ring and the DESY IV-based injector chain.

Timing System

Provides precise accelerator-related timing information and beam-synchronous signals and data:

- **Low-jitter machine clock signals** (derived from the 500 MHz RF reference)
- **Event-based trigger signals** (e.g. revolution and bunch triggers, beam injection/extraction
- **Operation-related information** (e.g. beam revolution number and timestamp; machine and beam status; bunch filling patterns; postmortem, injection veto and beam abort status).

Three central **Timing** and **RF synchronisation** systems are foreseen, one for PETRA IV, one for the DESY IV booster and LINAC II and one for the plasma-based injector, to cope with special operational modes (e.g. dispersion measurements) that require decoupling the activity of the storage ring from the injector chain. The systems re-synchronise after the special operational mode is completed.

Architecture of the PETRA IV Timing System

Comprises **central components** for PETRA IV and each one for the injectors with **multiple local systems** distributed in a star-like topology across the accelerator complex. The central sources broadcast the timing information to the local systems via a redundant, drift-compensated optical fibre network. The local timing systems either redistribute the timing information or provide it to accelerator subsystems and beamline experiments.

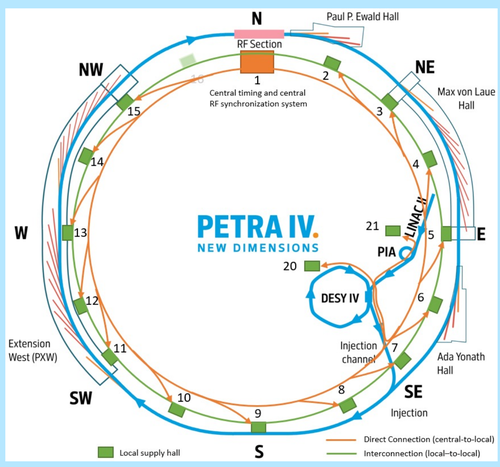
The **timing system** will be implemented based on the **MTCA.4** (Micro Telecommunications Computing Architecture) electronics standard, which was already successfully deployed and operated at the European XFEL and FLASH facilities.

Each **central** and **local** system consists of a 9U 12-slot **MTCA.4** crate equipped with:

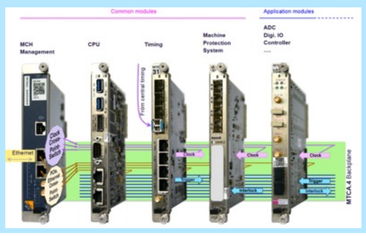
- **1 Host CPU AMC** (Advance Mezzanine Card)
- **1 MCH** (Management Controller Hub)
- **10 DAMC-X3TIMER** (main functional component)
- **10 RTMs** (optional)
- **2 Power Supplies** (redundant)
- **2 Cooling Units** (redundant)

The **DAMC-X3TIMER** modules are hardware-identical. They can be configured to operate as:

- **transmitters**, in central timing systems
- **repeaters**, in central/local systems for further distribution
- **receivers**, in local timing systems or MTCA.4-based accelerator/beamline client systems



Optical Fibre Distribution Topology

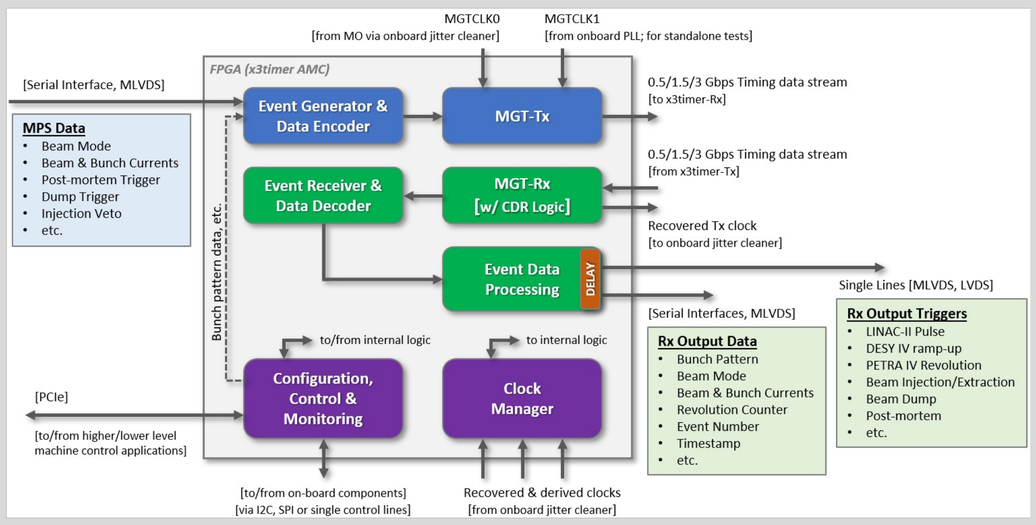


MTCA.4 Layout

Firmware Development - DAMC-X3TIMER Module

The firmware for the DAMC-X3TIMER will cover both receiver and transmitter functionalities. On the transmitter side, the device has to assemble and provide a **timing event block** and sent it serially via MGT-Tx links to the timing receivers, high-speed electrical links and optical fibre connections. The timer event block will comprise:

- Trigger information (e.g., dump trigger, postmortem trigger, injection veto) and machine configuration and status (e.g., beam mode, bunch pattern table, beam current) received from the MPS via a fast serial interface and from the machine control system via the local CPU and a PCIe interface;
- Locally generated trigger signals (e.g., triggers for the pre-accelerator chain, PETRA IV injection/extraction and revolution triggers);
- Locally generated timing data (e.g., revolution counter, bunch number, event timestamp).



DAMC-X3TIMER Firmware Functional Processes

Event data transmission will be driven by a low-jitter clock, derived from 500 MHz RF source of the synthesizer.

- Uses 8b/10b encoding w/ alignment characters.
- On-board clock and PLL for standalone mode.
- Baseline transmission rate of 0.5 Gbps w/ up to 3 Gbps option.
- Transmission clock will be recovered on every receiver and cleaned for jitter. Base for internal and external clock signals.
- Recovered event data with individual trigger events, signals and timing information.
- Global and local delays will be applied to all output serial links.
- FPGA configuration and monitoring via PCIe link to CPU.

Development uses DESY's Open Source Firmware Framework. See **MO4AO03,** The DESY Open Source FPGA Framework, by L. Butkowski.

Conclusions

For PETRA IV the timing and synchronisation system will be based on the successful implementation for the European XFEL to use efficiently synergies and readily available expertise across all accelerator facilities at DESY.

The new hardware development is based on the successful XFEL X2TIMER design with significant improvements on:

- **Short-term jitter reduction** by using a clock cleaner
- **Better drift stability**
  - Improved drift compensation
  - Usage of double-wavelength SFP/SFP+ transceivers
  - Thermal stabilization of board components
- **Enhanced, potential onboard processing capabilities**
  - More capable FPGA solution
  - Local control servers
  - Flexible configuration of peripherals

More flexibility through the use of in-house Open Source**software and firmware framework solutions**

- Interfacing to various **control systems**
- **Modular firmware** for easy portability

Firmware Framework
Project ID: 234

DOOCS.

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PETRA IV. NEW DIMENSIONS