ICALEPCS CAPE TOWN SOUTH AFRICA 2023

LEAPS INNOVATION

Scan me

TOWARDS DEFINING A SYNCHRONIZATION STANDARD BETWEEN BEAMLINE COMPONENTS AND SYNCHROTRON ACCELERATORS

Under the umbrella of LEAPS-INNOV project*, the Task 3 of Work Package 5 aims to define a standard for synchronization in the beamline sample environment. Their main partners (ALBA, DESY, DLS, ESRF and SOLEIL) have already reached a common vision of synchronization requirements. Trying to approach the utopic vision of a transparent synchronization integration of beamline parts with minimal effort and the reality of a experimental setup highly dynamic and diverse. The challenges of this work package come to fruition in 2 parts: Hardware synchronization device and a synchronization protocol.

Phases of the project

- Collate Existing Solutions and Future Requirements of Facilities for Beamline Synchronization (Done)
- Definition of the demonstrator Experiment for Beamline Synchronization (Done)
- Definition of a Standard Protocol for Synchronization between Beamline Components (On going)
- Installation of the Synchronisation Protocol and Demonstrator Experiment at several facilities (March'25)

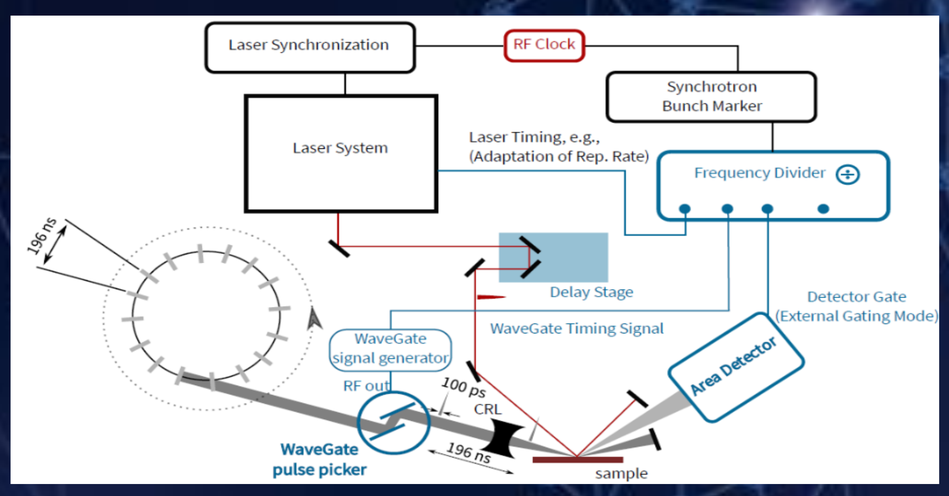

Fig.1: Demonstrator experiment

Synchronization Protocol

The project aims for the definition of a synchronization protocol to allow the description of the synchronization needs in all the ranges of time precisions. Moreover, it should be user-friendly for the experimenters, maybe with the use of a graphical tool, but also it must be simple to be interpreted by the SCADA systems and lately translated to the devices involved in the synchronization.

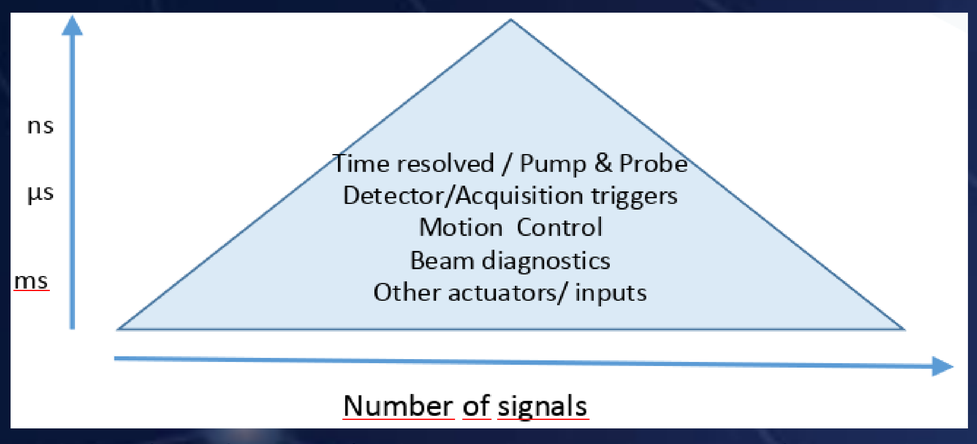

Fig.2: Relation between the time precision requirements and its quantity

Hardware

Many facilities have a real need of a synchronization equipment in the sample environment. As consequence, some of them have enrolled in the specification of it, coming to an agreement.

Name	*Input/ Output*	*Signal Type / Impedance*	*Form factor*	*Minimal Quantity*	*Optimal Quantity*	*Bandwidth (Hz)*	*Jitter (s)*
Interface #1 - DIFFIO	I / O	Diff / 120Ω (RS422)	DB15	4	8	50 MHz	1us
Interface #2 - DIO	I / O	Selectable LVTTL (TTL comp) / 50Ω / High-Z	Lemo 00	10	20	200 MHz	8ns
Interface #3 - DO	O	50Ω	Lemo 00	2	4	200 MHz	30ps (fine delay)
Interface #4 - EXP	IO	Vita 57.1	FMC LPC	1 (LPC)	2	FMC standard	NA
Interface #5 - OPT	IO	Fiber optics	SFP+	2	4	12.5Gbps	NA
Interface #6 - ETHERCAT	I/O	Ethernet	RJ45	1	1	10GBps	NA
Interface #7 - MNGMNT	IO	RS232, JTAG, USB, ETH etc.	DB9, JTAG, USB, RJ45 …	2 (RS232, ETH)	4 (All)	Standard	NA
Interface #8 - AI	I	Analog Input Range selectable [+/-1V, 0-5V], Hi-Z	BNC	0 (Optional on FMC)	8	1MHz ADC, 16bit	NA
Interface #9 - AO	O	Analog Output Range [+/-10V], 1kOhm	BNC	0 (Optional on FMC)	4	1MHz DAC, 16bit	NA
Interface #10 - CLKIN	I	RF Clock Input	SMA	0 (Optional on FMC)	1	500MHz	20ps
Interface #11 - CLKOUT	O	RF Clock Output	SMA	0 (Optional on FMC)	1	500MHz	20ps

Table.1: Final specification proposal for HW I/O interface

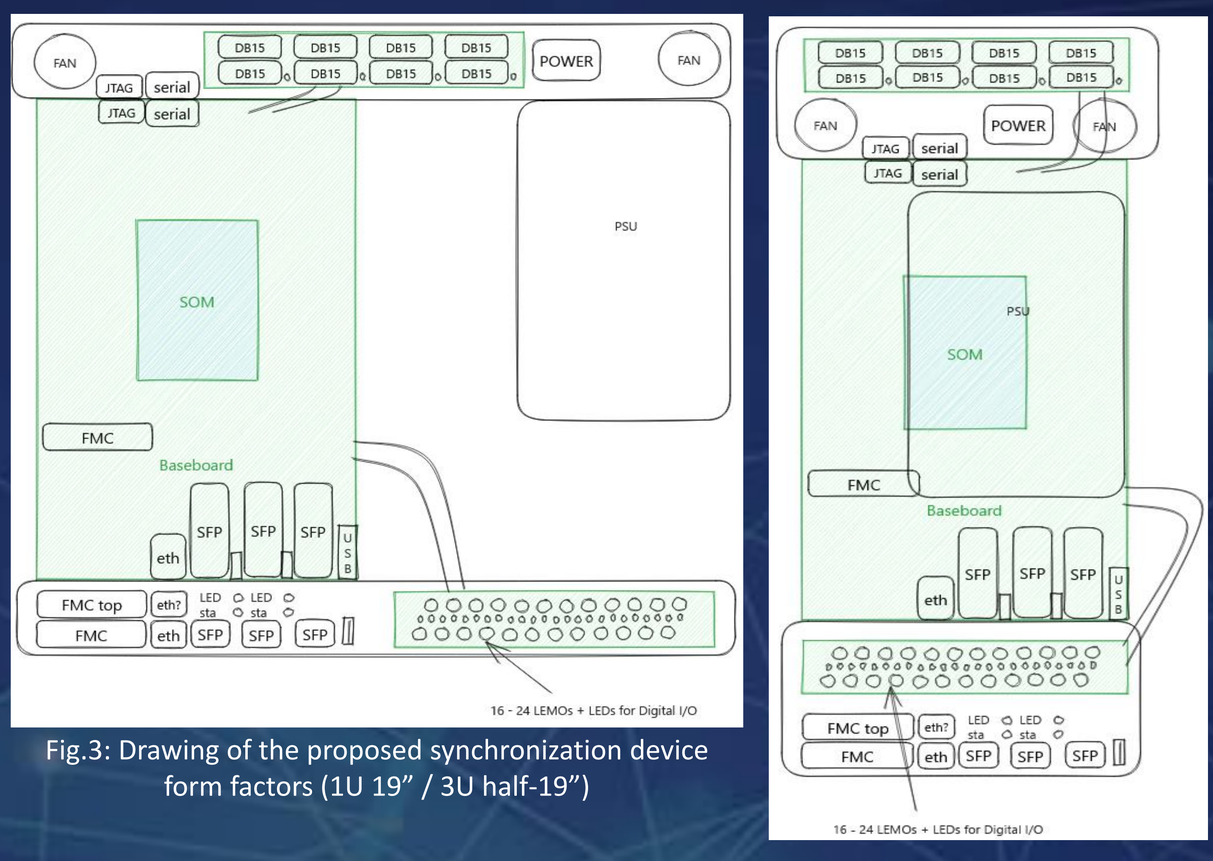

Fig.3: Drawing of the proposed synchronization device form factors (1U 19" / 3U half-19")

This project has received funding from the European Union´s Horizon 2020 research and innovation programme under grant agreement no. 101004728.

* https://leaps-initiative.eu/