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CONTROL SYSTEMS DESIGN FOR STS ACCELERATOR*

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Abstract

STS accelerator systems will build a Ring-to-Second-Target (RTST) transport beamline from the present Ring to Target Beam Transport (RTBT) to the second target. The integrated Control Systems (ICS) will provide remote control, monitoring, OPI, alarms, and archivers for the accelerator systems, such as magnets power supply, vacuum devices, and beam instrumentation. The ICS will upgrade the existing Linac LLRF controls to allow independent operation of the FTS and STS and support different power levels of the FTS and STS proton beam. The ICS accelerator controls are in the phase of preliminary design for the control systems of magnet power supply, vacuum, LLRF, Timing, Machine Protection System (MPS), and computing and machine network. The accelerator control systems build upon the existing SNS Machine Control systems, use the SNS standard hardware and software, and take full advantage of the performance gains delivered by the PPU Project and SNS.

INTRODUCTION

The Second Target Station (STS) Project includes the comprehensive design, construction, installation, and commissioning of the essential facilities and equipment aimed at establishing a cutting-edge source of cold neutrons with unprecedented peak brightness at the Spallation Neutron Source (SNS). The project leverages the capacity of the existing SNS accelerator, accumulator ring, and infrastructure and takes full advantage of the performance gains delivered by the Proton Power Upgrade (PPU) Project [1]. The PPU will double the SNS proton beam power from 1.4 MW to 2.8 MW. This increase is achieved by integrating seven additional superconducting cryomodules into the existing linear accelerator (Linac), resulting in a 30% rise in beam energy combined with a 50% rise in beam current. Operating at a frequency of 60 Hz, the SNS accelerator, when combined with the STS, will supply 45 pulses per second to the First Target Station (FTS) and 15 pulses per second at a frequency of 15 Hz to the STS. STS Accelerator Systems will build a new 231.9-meter-long Ring to Second Target (RTST) beamline to transport protons from an extraction point in the existing Ring to Target Beam Transport (RTBT) line to the Second Target. The RTST system integrates diverse components, including vacuum systems, magnets, power supplies, beam instrumentation and diagnostics, and utilities, all working in tandem to support its operation. This paper describes the integrated controls of the STS accelerator systems.

STS ACCELERATOR CONTROLS

STS Accelerator Control systems build upon the existing Experimental Physics and Industrial Control System (EPICS) SNS Control systems, effectively utilizing SNS standard hardware and software components where applicable to govern the operation of the RTST [2]. The purview of the Accelerator Controls encompasses an array of vital aspects, including vacuum controls, magnet power supply controls, the Machine Protection System (MPS), the Run Permit system (RPS), the Timing system, core software, machine networking and computing, and upgrades to the Low-level Radio Frequency (LLRF) control for the pre-existing Linac.

Vacuum Controls

The RTST vacuum system will extend the vacuum configuration from the existing RTBT to the STS. This comprehensive system comprises various crucial elements, such as vacuum assemblies, sensors, pumps, and associated instrumentation, which include valves, gauges, gauge controllers, and pump controllers. To effectively regulate and monitor the vacuum equipment within the RTST, a dedicated vacuum control system has been devised. The architecture of this control system is modelled on the well-established RTBT vacuum control system, which is grounded in the utilization of Allen-Bradley (AB) Programmable Logic Controllers (PLCs) and EPICS Soft Input/Output Controllers (IOCs) [3]. Specifically, an Allen-Bradley ControlLogix PLC will be deployed to oversee gauge and pump operations, control vacuum valves, and provide interlocking to the Machine Protection System (MPS). Communication between the PLC and the EPICS IOCs will be facilitated via EtherNet/IP [4], while Linux workstations will serve as the operator interface.

Magnet Power Supply Controls

The 15 Hz beam will be extracted from the RTBT, directed to the RTST using pulsed dipole magnets, and then transported to the second target with quadrupole, dipole, and corrector magnets. Both DC magnet power supplies and pulsed dipole power supplies are utilized to provide the necessary current for all these magnets. The control interface for the DC magnet power supplies is established through Ethernet or serial communication protocols. The EPICS control software will be developed to control all power supplies. Furthermore, an interlock system will be implemented between the power supply and the Machine Protection System (MPS).

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For the extraction of the STS beam, four specialized pulsed dipole magnets, designed by Fermilab (FNAL), will be strategically installed. Each of these magnets will be powered by a commercial Magnetic Resonance Imaging (MRI) gradient power amplifier. These power amplifiers necessitate a comprehensive control solution to generate and monitor pulse waveform effectively. The accompanying Figure 1 provides a visual representation of the block diagram illustrating the RTST Extraction pulsed dipole waveform generator and waveform monitor system.

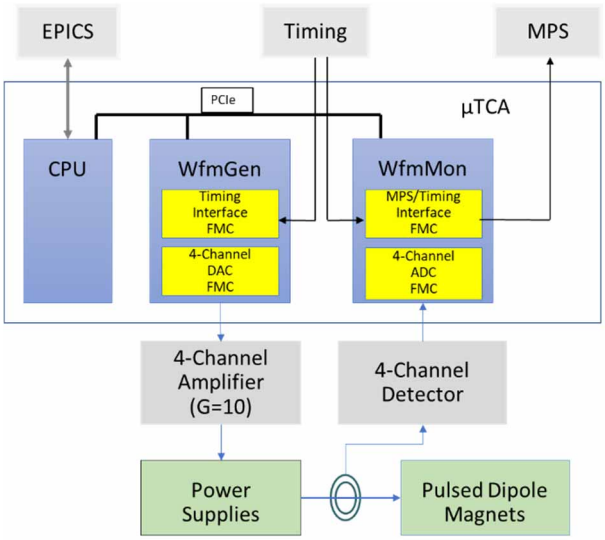

Figure 1: The Block Diagram of the RTST Extraction Pulsed Dipole Waveform Generator and Monitor

The Waveform generator and waveform monitor system are built upon the MicroTCA platform, running a Linux-based operating system. The waveform generator comprises a Vadatech AMC502 dual FPGA (field-programming gate array) Mezzanine Card (FMC) carrier, along with a timing interface FMC and a 4-channel Digital-to-Analog Converter (DAC) FMC. Its primary function is to receive timing information related to the second target pulse and subsequently generate excitation ramp-up signals for the power supplies. On the other hand, the waveform monitor is equipped with a single AMC502 FMC card, housing both a timing interface card with additional output to the MPS, and a 4-channel Analog-to-Digital Converter (ADC) FMC. Its role involves sampling the readback current signals from the power supplies and conducting validation of the current waveform. If the current waveform deviates beyond the predefined upper and lower operation thresholds, the system promptly notifies the MPS through the output on the timing interface card. The waveform monitor samples the readback current signals from the power supplies and validates the current waveform. If the current waveform falls outside the operator-defined upper and lower bands, the MPS will be notified via the timing interface card.

Timing System

STS timing system is an extension of the existing SNS timing system, which serves to synchronize the operation of the LINAC, accumulator ring, and neutron instruments, while also distributing timing events, and machine data to accelerator systems, target systems, and instrument data acquisition systems. Operating in a unidirectional manner, the SNS Timing System originates from the Timing Master and broadcasts to various timing clients across the SNS site. It's composed of two serial transmission links: the Event Link (EL) and the Real-Time Data Link (RTDL). The Event Link conveys 8-bit timing events defining SNS Machine Cycle segments. The RTDL transmits 24-bit data frames that specify machine operating parameters preceding a machine cycle. The Single Link (SL) combines EL and RTDL, transmitting timing events and RTDL frames in a single fiber to timing receivers. The STS Timing system extends SNS timing distribution links to STS timing receivers. The block diagram of STS timing system interfaces is illustrated in Figure 2. STS timing system receives timing information from the SNS Timing master and distributes it to Linac LLRF, RTST beam instrumentation and diagnostics, RTBT to RTST extract pulsed dipoles, PPS, Target controls, and instrument controls and DAQ.

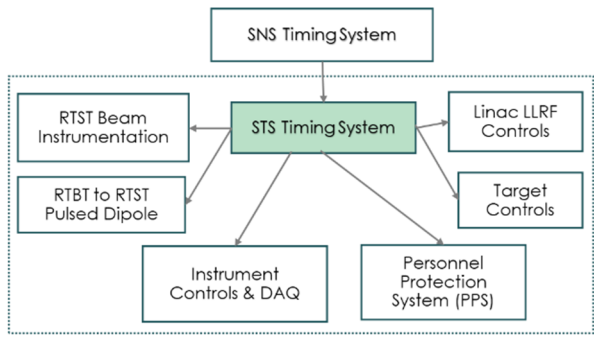

Figure 2: The Interface of the STS Timing System

Within the STS context, the timing system is mandated to support both single and dual target station operations. This encompasses autonomous beam power ramping for each target and independent control of both FTS and STS beams. While FTS and STS beam pulses are provided by the same accelerator and thus have the same beam energy, they operate at separate rates and may carry different beam charges, resulting in the desired beam powers. These two beam types refer to two beam flavors: the 'FTS beam flavor' and the 'STS beam flavor.' To accommodate these two beam flavors, the events and RTDL of the SNS Timing system will necessitate updates. Keeping the existing timing system technology, events and RTDL data that originally referred to the SNS beam will be specialized to address FTS beam pulses. Previously unused events and RDTL data frames will provide information for STS beam pulses. To validate these events and RTDL frames, a VME Timing Master test stand was constructed. Figure 3 shows the picture of the Timing Master test stand. The setup consists of a VME processor, a Timing Master card, and a function generator simulating the Ring Clock. The firmware event

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tables and timing system timeline were corroborated using timing system software and an oscilloscope. Support for STS operation was demonstrated solely via updates to the timing master software. The Timing Master hardware and firmware for STS operation remains entirely compatible with operational SNS software. At the preliminary design stage, only eleven new events and two added RTDL frames suffice to support FTS, STS, and combined FTS/STS operations.

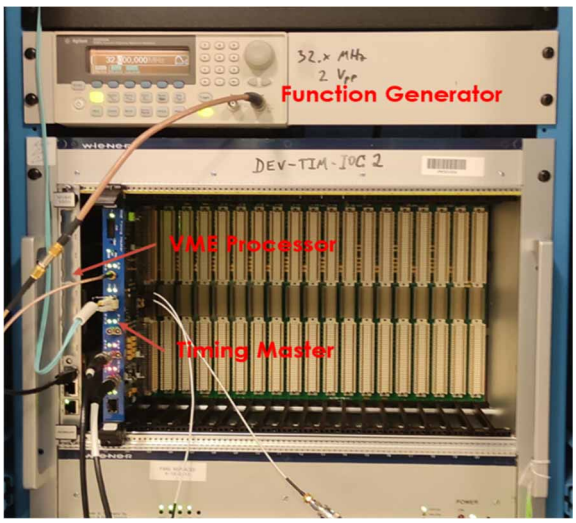

Figure 3: The STS Timing Master Test Stand

Run Permit System (RPS)

The RPS is a high-level software tool that helps operators coordinate the independent beam delivery to the FTS and STS. This powerful tool grants operators the ability to enable and disable the beam for either or both target stations while maintaining precise control over the pulse rate directed to each station. Figure 4 illustrates various operating scenarios for FTS and STS beam modes. Within the framework of SNS accelerator operations, the base rate is set at 60Hz. In Scenario (a), all pulses are delivered to the FTS at a nominal rate of 60Hz, representing the primary operating mode before the STS phase. To allow STS operation, every 4th machine cycle will be reserved for STS pulses. Scenario (b) shows the STS running at a nominally 15 HZ, while the FTS operated with 45 pulses per second. Scenario (c) involves the deactivation of the FTS, with the accelerator solely generating beam pulses for the STS at its maximum rate of 15 Hz. Scenario (d) demonstrates both the FTS and STS operating at their highest achievable interleaved rate of 45 pulses per second and 15 Hz, respectively, with the STS utilizing a reduced pulsed power by lowering the beam charge in each STS pulse compared to the STS pulses.

The RPS interfaces seamlessly with multiple systems, including the Timing system, the MPS, and the LLRF system. It translates the operational mode requests for interleaved beam delivery to the two target stations into the requisite configuration settings for these systems. Several existing SNS subsystems require updates to support the full implementation of the RPS. The MPS plays a pivotal role in defining the SNS operating mode on a pulse-by-pulse basis, which includes a combination of machine mode and beam mode. To accommodate STS operations, a set of new MPS modes will be assigned. When both target stations are in use, the MPS mode will alternate between referring to the FTS and the STS during each machine cycle. Within this framework, the Timing master employs the RTDL and event link to transmit critical information, such as MPS mode, beam flavor, 'beam on' events, and more, to each timing system client across the facility. The RPS assumes the responsibility of computing the schedule for the 10-second supercycle and consistently populates the event table in the timing master to orchestrate beam delivery to the FTS, STS, or both, in accordance with operational requirements.

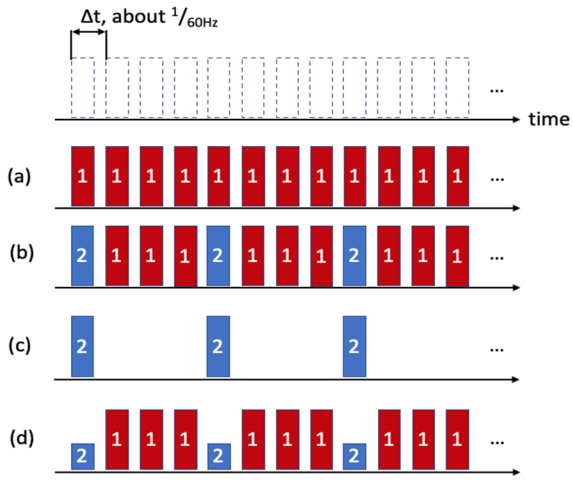

Figure 4: Accelerator Operating Modes for FTS 1 and STS

Machine Protection System (MPS)

The SNS Machine Protection System (MPS) has undergone a significant upgrade, incorporating commercial µTCA hardware into its design. This upgraded system now boasts a distributed architecture, comprising a master controller, fiber link infrastructure, and field nodes. The master controller configuration includes a µTCA chassis housing a processor (IOC), crossbar switch, node processors, and trigger control mechanisms. Its primary role is to swiftly disable beam generation in response to any qualified fault reported from a downstream node, thereby ensuring the safety and integrity of the accelerator. Each field node is housed in a compact 1U µTCA chassis and is equipped with an AdvancedMC module (AMC) and a Rear Transition Module (RTM). These field nodes monitor sensors on low-level devices and establish communication with the node processors. Each field node monitors 32 channels. Each node processor communicates with up to 8 field nodes. With a maximum of 10 node processors in the master controller, the system can handle about 2500 channels. Before STS, SNS uses less than half of the available MPS channels. The STS MPS extends the pre-existing SNS MPS, harnessing the capabilities of µTCA hardware to accommodate additional field nodes dedicated to the STS

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systems. Figure 5 provides an overview of how the MPS interfaces with these crucial systems, highlighting its integral role in ensuring their reliable operation and protection.

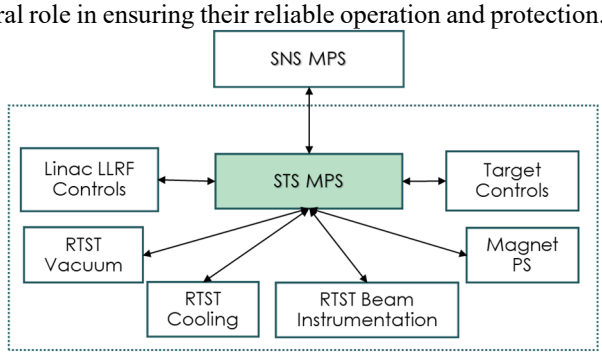

Figure 5: STS MPS Interface with Other STS Systems

Linac LLRF Controls

The Linac LLRF Control system will be upgraded to facilitate the independent operation of both the FTS and STS, accommodating distinct power levels of their respective proton beams. Due to constraints such as component obsolescence and limited backplane bus bandwidth, the existing LLRF systems cannot meet the demand to support two beam flavors. To address this, the STS project necessitates the replacement of 96 original Linac LLRF systems using the hardware design of the PPU LLRF system based on the µTCA platform [5]. During this upgrade, the existing racks will be retained, but the original VXI crates and down converters will be supplanted by µTCA crates and Frequency Conversion Chassis (FrCC) chassis. The major hardware components of the PPU LLRF system are µTCA.4 chassis, processor card (or IOC), timing module, Field Control module II (FCM-II), and High-power Protection module II (HPM-II). The project entails the installation of a total of 55 new µTCA crates and the replacement of 96 LLRF systems. The significant hardware components for the STS project are itemized in Table 1

Table 1: STS LLRF Major Hardware Components

Component	Device Type	Quantity
µTCA Crate	VadaTech VT815	55
Shelf Manager	UTC002	55
Processor Card	AMC716	55
Timing Module	AMC502 +	55
	FMC	96
Timing Fanout	TiFFF	8
FMC II	AMC523+MRT523B	96
HPM II	AMC523+MRTHPM	96

The PPU Project has developed Linux EPICS software for the LLRF µTCA IOCs. Currently, the software supports the FTS operation only. STS Accelerator Controls will update the software to support both FTS and STS two-beam flavors operation by adding a second beam compensation buffer for the STS. The EPICS OPI screens will be modified to match the hardware status and two-beam flavors operation while remaining compatible with the existing system.

CONCLUSION

The STS Project has received DOE approval for Critical Decision 1 which defines the project cost range and allows preliminary design work. The cost and schedule for ICS Accelerator Control systems have been well defined, and the preliminary design for the subsystems is under development. Some systems, such as the Timing system, Run Permit system, Linac LLRF Controls, Core software, and Machine network, have finished the preliminary design review, and are ready for the final design. Based on the operation of existing SNS control systems and taking full advantage of the success of the PPU Project, the STS ICS Accelerator Control systems design is right on track for the next milestone of the STS Project.

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