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DEVELOPMENT AND TEST OPERATION OF THE PROTOTYPE OF THE NEW BEAM INTERLOCK SYSTEM FOR MACHINE PROTECTION OF THE RIKEN RI BEAM FACTORY

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Abstract

Since 2006, we have been operating a beam interlock system (BIS) for machine protection at the RIKEN RI Beam Factory (RIBF). The system has a reaction rate of approximately 15 ms after receiving an alert signal from the accelerator and beamline components. Considering that the beam intensity of the RIBF will increase, we are currently developing a successor system to stop the beam within 1 ms. After comparing multiple systems, CompactRIO, a National Instruments product, was selected as the successor system. Interlock logic for signal input/output is implemented on a field-programmable gate array (FPGA) to ensure fast processing speed. However, signal condition setting and monitoring do not require the same speed as the interlock logic. Therefore, they are implemented on a real-time operating system (RT-OS) and controlled using the Experimental Physics and Industrial Control System (EPICS) by setting up an EPICS server on the RT-OS. Furthermore, in the successor system, a system for fast alert signals, such as digital signals, immediately outputs from the equipment. In addition, a system for slow alert signals, such as analog values of the beam current sampled at a certain period, is developed as a linked system. Development of the successor system began in 2021. As of the summer of 2023, a prototype consisting of three stations for processing digital input signals and one station for processing analog input signals was installed in parallel with part of the BIS. The time required for the prototype to output a signal required to stop a beam after receiving an alert signal averaged 130 μs for a digital input signal and 470 μs for an analog input signal. These results show that the prototype can achieve much better performance than the target system response time, and the target performance can be expected to be achieved when the prototype is extended to the entire system in the future.

INTRODUCTION

The RIKEN Radioactive Isotope Beam Factory (RIBF) at the RIKEN Nishina Center for Accelerator-Based Science is a complex accelerator facility comprising multiple linear accelerators, including a superconducting linac, multiple cyclotrons, and the world's largest superconducting cyclotron. Furthermore, RIBF can provide the world's most intense RI beams over the entire atomic mass range using the fragmentation or fission of high-energy heavy ions [1].

The components of the RIBF accelerator complex (such as the magnet power supplies, beam diagnostic devices, and vacuum systems) are controlled by Experimental Physics and Industrial Control System (EPICS) [2]. However, exceptions exist, such as the control system dedicated to the RIBF's radio frequency system [3]. All essential operation datasets of EPICS and other control systems were integrated into an EPICS-based control system [4]. Two independent safety systems operate in RIBF facilities: a radiation safety interlock system for human protection [5] and a machine protection interlock system [6].

OVERVIEW OF THE THREE TYPES OF BEAM INTERLOCK SYSTEMS IN OPERATION

RIBF currently has three machine protection interlock systems: the beam interlock system (BIS), AVF-BIS, and superconducting RIKEN Linear Accelerator (SRILAC)-BIS. First, the BIS is the largest of the three abovementioned beam interlock types and began operation in 2006. It was developed based on Melsec-Q series programmable logic controllers (PLCs), a product of the Mitsubishi Electric Corporation [7]. Figure 1 shows the hardware configuration and process flow of the BIS. Furthermore, it was designed to stop the beams within 10 ms of receiving an alert signal from the accelerator and beamline components. Upon receiving an alert signal, the BIS outputs a signal to one of the beam choppers, which immediately deflects the beam downstream of the ion source (the time required for this is called the system response time). It also inserts a beam stopper (Faraday cup) installed upstream of the problematic component. The BIS ignores the problems that occur downstream of the beam stopper insertion point. After inserting the relevant beam stopper, the beam chopper can be switched off, and beam delivery can resume up to the inserted beam stopper. This feature is particularly important because the problem recovery time can be effectively used to readjust the beam to the inserted beam stopper when the problematic component cannot be recovered within a short time. Moreover, the inserted beam stopper can be extracted from the beamline after the problem is resolved.

The BIS consists of five PLC stations with 384 digital inputs (DI), 80 digital outputs (DO), and 112 analog inputs

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(AI). Two sets of BIS with the same specifications monitor almost all the components of the RIBF accelerators except the components monitored by AVF-BIS and SRILAC-BIS. The reasons for installing two sets of the same system were as follows. The RIBF facility monitored by the BIS is divided into two parts: a new facility that began operations in 2006 and an old facility that has been in operation since then; the new facility is operated in conjunction with the old facility. Originally, the BIS was developed as a system for new facilities. Subsequently, when updating the safety system of the old facility for machine protection, the BIS should have been expanded. However, expanding the system would slow the signal response time of the BIS. Therefore, another set of BIS with the same specifications was installed in the old facility.

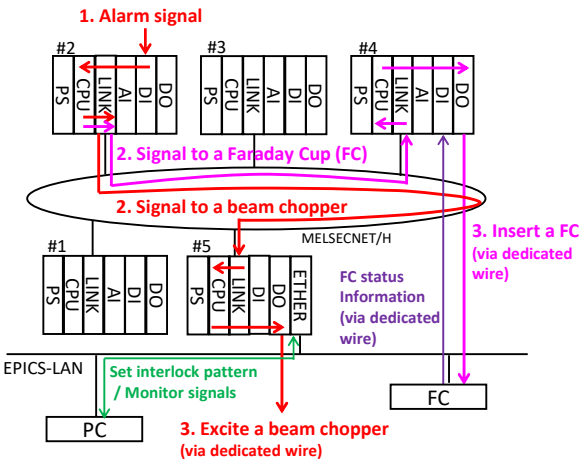

Figure 1: Example of the hardware configuration and process flow in the BIS. ETHER means Ethernet module, and LINK means Melsec Link Module.

After more than 10 years of operation, the BIS is still under stable operation; however, its maintenance has gradually become difficult. For example, some modules used in the system were discontinued and could not be replaced. Furthermore, the performance of the system has been declining owing to the increasing interlock signal input to the system during RIBF operation. Considering the above, we began developing a new machine protection interlock system in 2016 using FA-M3 series PLCs manufactured by Yokogawa Electric Corporation [8], which implements the same interlock functions as the BIS. One advantage of this system is that it can adopt a multi central processing unit (CPU) configuration. The system response time can be reduced by using different types of CPUs according to the speed required for each process. These processes include stopping the beam after receiving an alarm signal or parameter setting and monitoring the system. In 2020, we developed two sets of prototypes consisting of two stations. We installed them in two locations: one in the AVF cyclotron and its low-energy experimental facility as AVF-BIS and the other in the RILAC and SRILAC experimental facilities as SRILAC-BIS. Figure 2 shows the hardware configuration and process flow of the AVF-BIS. AVF-BIS has two stations and implements 64 DI, 28 DO, and 24 AI. Both stations implemented a CPU and communicated via Ethernet. In contrast, a dedicated FL-net [9] is used to share the status of the DO signals. The system response time of the AVF-BIS averaged 5.4 ms with both stations (the distance between the two stations is approximately 70 m) [10].

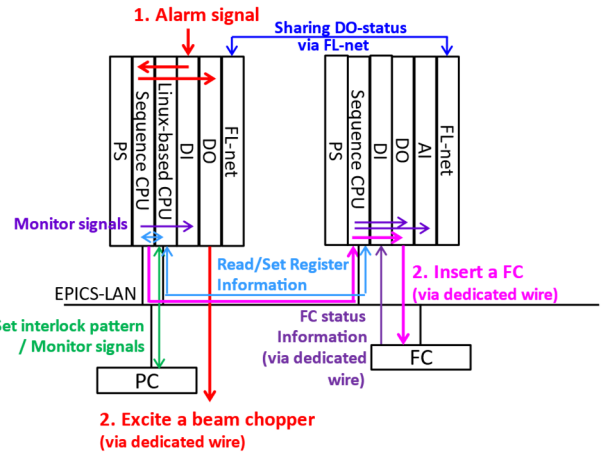

Figure 2: Hardware configuration and process flow in the AVF-BIS.

In contrast, the SRILAC-BIS is a system that has gradually improved and expanded upon the prototype. Figure 3 shows the hardware configuration and process flow of SRILAC-BIS. It has one main station and seven substations, and each station has either 32 or 56 DI, either 32 or 56 DO, and 8 AI. The main station with the installed CPU module communicates with the seven stations via an optical FA bus. One of the features of SRILAC-BIS is that it implements a high-speed input/output (I/O) module with a field-programmable gate array (FPGA) (F3DF01) [11] in addition to the regular I/O module. This allows SRILAC-BIS to respond quickly when an anomaly is detected in the superconducting cavity of the SRILAC. The system response time when a signal is input to the standard DI module of a sub-station is approximately 6 ms, and to the F3DF01 of the main station is approximately 78 μs [12].

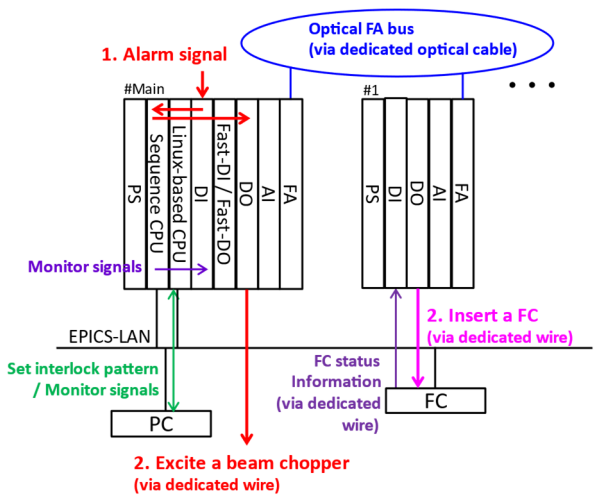

Figure 3: Hardware configuration and process flow in the SRILAC-BIS. FA means optical FA bus module.

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DEVELOPMENT, IMPLEMENTATION, AND CURRENT STATUS OF THE NEW BIS SYSTEM

Based on the operational data of the AVF-BIS, we estimated the system response time to be less than 10 ms when expanding the prototype to the scale of the BIS. Considering the possibility that the beam intensity accelerated by the RIBF will continue to increase and require the monitoring of more components in the future, a simple expansion of this prototype will possibly no longer meet our performance requirements. Therefore, we considered two alternatives for the successor system of the BIS: one was to introduce FPGA modules into the FA-M3-based system as in SRILAC-BIS, and the other was to develop a new system based on CompactRIO [13], a product by National Instruments. As a prerequisite for consideration, the BIS should monitor much more equipment than the SRILAC-BIS and cover various operation modes that are more complicated than the SRILAC-BIS. For example, the total number of magnet power supplies monitored by the SRILAC-BIS is 134, whereas the BIS monitors 740. In addition, the beams were transported in only one direction in a facility covered by the SRILAC-BIS. In contrast, in a facility covered by a BIS, beams may be transported in opposite directions along a beam transport line, depending on the operation mode selected for the experiment. Therefore, the successor system must easily and flexibly adapt to complex operating patterns and should not be expensive. As for the CompactRIO features, we can develop complex FPGA logic relatively easily using LabVIEW, which is intuitive and easy to understand [14]. Furthermore, in a system with many inputs, such as a BIS, the total cost of a system with CompactRIO, where the FPGA is mounted in the chassis, is lower than that of a system with F3DF01, where the FPGA is mounted in the module. Consequently, we selected CompactRIO and began the development of a successor system with the same interlock logic as the existing BIS in 2021 (hereafter referred to as the successor system RIBF-BIS2). Because the RIBF-BIS2 implements an FPGA, we aimed to develop it with a system response time of 1 ms or less.

The CompactRIO system has three layers for implementing logic for signal control: the FPGA layer, which is the most reliable and capable of the fastest signal processing; a real-time operating system (RT-OS) layer, which is positioned in the upper layer of the FPGA and communicates with the FPGA; and a Windows OS layer, which is positioned in the upper layer and communicates with them. The system response time must be as short as possible; thus, the interlock logic for the signal I/O is implemented on the FPGA. However, signal condition setting and monitoring do not require a fast response time, similar to interlock logic processing; thus, they are implemented on the RT-OS and controlled using EPICS by setting up an EPICS server.

Figure 4 shows the hardware configuration and process flow concept of RIBF-BIS2. The RIBF-BIS2 stations were designed to be installed at the same location as the BIS, and the existing signal wiring from each device was to be reused. To realize the interlock logic of the BIS, we developed two types of logic units: the BIS Logic Unit (BLU) and the BIS Chopper Unit (BCU) using I/O modules. The BLU judges conditions such as the mask and holding time for each alert signal input and sends a signal to the BCU that requires the excitation of a beam chopper via a dedicated hard wire. The BCU compares the input signal from the BLU and the insertion status of the Faraday cup and outputs a signal to the beam chopper when necessary. The station implementing BLU is installed near the controller that outputs alert signals from each equipment (#DI-1 to #DI-9 and #AI-1 to #AI-7 in Fig. 4), and the station implementing BCU is installed at the console (#Chopper in Fig. 4).

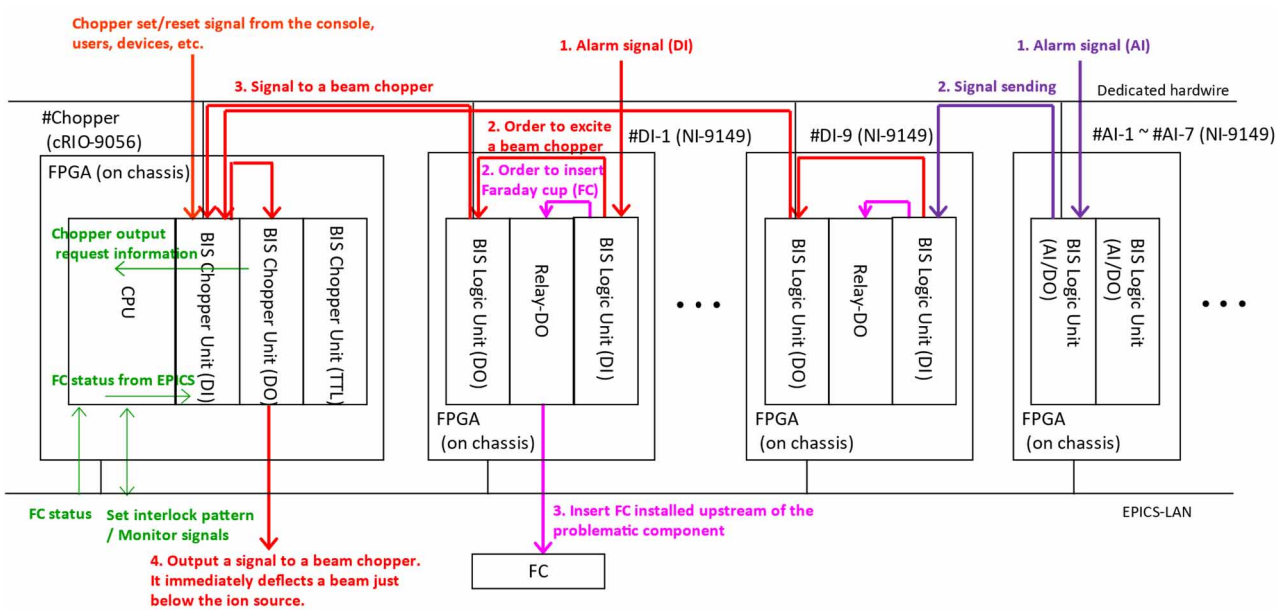

Figure 4: Hardware configuration and process flow in the RIBF-BIS2.

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Based on operational experience with the BIS, we improved several specifications for developing RIBF-BIS2. The first improvement was the separation of the input signals by signal type. Two types of signals are connected to the BIS: the instantaneous signal output from the equipment when an anomaly occurs and the signal output when the analog value, such as the beam loss current detected by the baffle slit of the cyclotrons, exceeds a certain threshold value. The latter case is not expected to detect anomaly as quickly as the former case due to the characteristics of the log amplifiers used to detect the beam loss current as well as the fact that the logic of comparing analog input values to threshold values is required to determine abnormalities. However, the BIS mixes a module for AI signals and a module for DI signals at the same station, and one CPU at each station processes both signals. In the RIBF-BIS2, we separate them into two parts to respond to the former signals within the fastest time. Stations dedicated to analog signal processing (hereafter, the AI Station) and stations dedicated to digital signal processing (hereafter, the DI Station) were installed. As shown in Fig. 4, an alert to an AI Station is output as a DO signal from the AI Station, and the DO signal is input to the DI Station via a dedicated wire to stop the beam. The second improvement combines the two sets of BISs into a single system. As the parts of a facility currently covered by two sets of BIS often operate as a single facility, it would be more efficient to unify the system.

In RIBF-BIS2, all of the DI Stations will be implemented 192 DI except for the chopper station, and the logic to be executed in the FPGA will be common at every DI Station. Considering that the number of terminals for DI signals at each station of the BIS is either 64 or 96, this specification should be sufficient, even if new equipment is introduced or facilities are expanded in the future. In contrast, all AI Stations of the RIBF-BIS2 will be implemented at 64 AI. The number of terminals for the AI signals at each station of the BIS is either 16 or 40; this specification should also be sufficient.

First, we set up a prototype for DI signals using one CompactRIO chassis and one expansion chassis with I/O modules and started the development of the logic in 2021. Table 1 shows the modules used in the prototype. After completing the development of the prototype in the control room, it was installed in part of the RIBF during the summer of 2022. The CompactRIO chassis of the prototype was installed as a chopper station, and the expansion chassis was installed as a DI Station 1. Because the prototype was planned to be tested in a part of the BIS consisting of five stations, we connected the input signals to the prototype in parallel with the BIS. The GUI for signal settings and monitoring of the prototype was developed using the Control System Studio (CSS) [15] of EPICS, and COEIROINK: TSUKUYOMI-CHAN [16] was used for audio when an anomaly occurred. The log system was developed based on the system used in the RILAC operation [17].

Table 1: Modules in the Prototype

Module	Type	Quantity
CompactRIO Station		
cRIO-9056	Chassis	1
NI-9426	DI	5
NI-9475	DO	1
NI-9401	5V TTL	1
Expansion Chassis Station		
NI-9149	Chassis	1
NI-9426	DI	6
NI-9477	DO	1
NI-9485	Relay DO	1

After the prototype was installed, we measured the response time of the system with alert signals generated experimentally from the actual component. We obtained a result of 520 µs (average of five measurements). The distance between the chopper station and the DI Station 1 is approximately 75 m. Furthermore, it was confirmed by the test that the response time can be reduced to 129.4 µs (average of five measurements) by adding a pull-up circuit, which consists of a constant-current diode and LED in parallel to the signal input part. Therefore, we decided to install a pull-up circuit at each input section for all DI signals. Because the response time of the BIS measured using the same signal was approximately 15 ms, we developed a system that was approximately 100 times faster than the BIS.

We started the test operation of the prototype during the beam service times scheduled for the latter half of the 2022 fiscal year. Minor corrections were necessary; however, no major defects were observed. Therefore, we took the next step in developing the logic for the AI Station. The logic of the AI station is the same as that of the BIS, in which we used two threshold values: the upper limit and the "upper-upper" limit values. The former corresponds to a warning and the latter to an anomaly. Considering the possibility that AI values other than the beam loss currents may be input to the system, RIBF-BIS2 expanded the logic to allow setting a lower limit value and a "lower-lower" limit value smaller than the lower limit value. The AI station outputs only a warning sound when the input value exceeds the upper or lower limits and outputs a signal requesting the beam to stop when the input value exceeds the "upper-upper" or "lower-lower" limits.

We expanded the above prototype by adding one DI Station and one AI Station to BIS Station 2 during the summer of 2023. Table 2 lists the modules used at Station 2. After expanding the system, we measured the response time using the DI signals generated experimentally from one of the actual components and obtained an average of approximately 129.0 µs. In contrast, the response time of the AI Station was approximately 470.3 µs. The input signal for the AI Station, a pulse signal generated by a function generator was experimentally input for measurement. The measurement results obtained using the oscilloscope are shown in Fig. 5 and Fig. 6. The distance between the chopper station and station 2 was approximately 135 m.

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Table 2: Modules at Station 2

Module	Type	Quantity
cRIO-9056	Chassis	1
NI-9205	AI / DO	2
NI-9149	Chassis	1
NI-9426	DI	6
NI-9477	DO	1
NI-9485	Relay DO	1

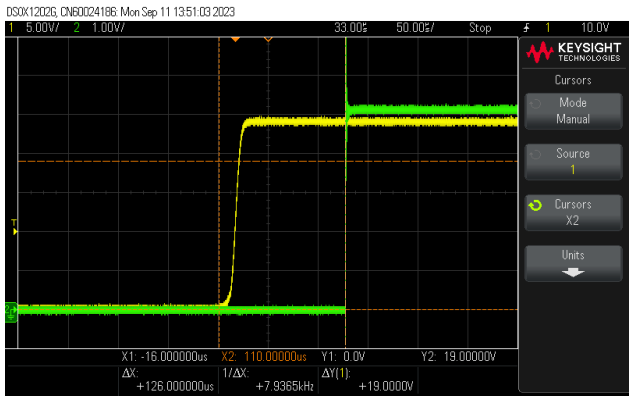

Figure 5: Signal output timing at RIBF-BIS2 DI Station (129.0 µs in average). The yellow and green lines represent the input and output signals, respectively.

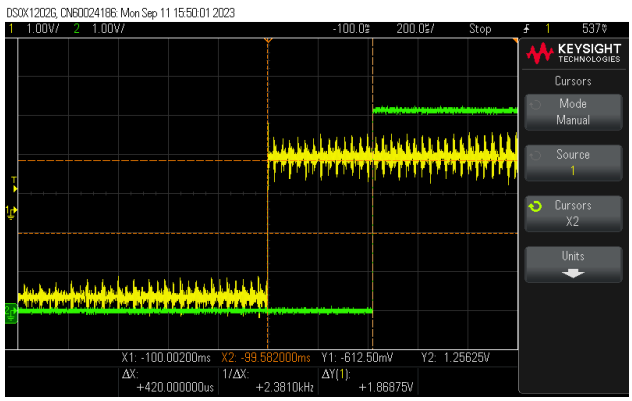

Figure 6: Signal output timing at RIBF-BIS2 AI Station (470.3 µs in average). The yellow and green lines represent the input and output signals, respectively. Pulses are output from a function generator at a 10 kHz cycle.

Because there was no major change in the response time before and after the system expansion, we will continue expanding the prototype and plan to replace the BIS with RIBF-BIS2 within 2 years. However, there is currently one concern regarding the management of shared variables on the EPICS server of the RT-OS. Because we used EPICS for all condition settings and monitoring signals connected to the system, the EPICS server managed several times as many shared variables as the signals. Currently, the DI system has approximately 1300 shared variables for the chopper station and the two DI Stations. The AI system has approximately 530 shared variables for one station. In the current system design, the DI system consists of 10 stations, and from a cost perspective, one CompactRIO chassis and nine expansion chassis are required. In contrast, the AI system is planned to consist of one CompactRIO chassis and six expansion chassis. These shared variables increased proportionally with the number of stations. Because the expansion chassis does not have an RT-OS and cannot implement an EPICS server, we may need to install a CompactRIO chassis instead of an expansion chassis to increase the number of EPICS servers.

REFERENCES

[1] O. Kamigaito *et al.*, "Recent progress in RIKEN RI Beam Factory", in *Proc. Cyclotrons 2019*, Cape Town, South Africa, Sep. 2019, paper MOB01, pp. 12-16. doi:10.18429/JACoW-Cyclotrons2019-MOB01

[2] EPICS, https://epics.aps.anl.gov

[3] M. Komiyama *et al.*, "Recent improvements to the RIKEN RI Beam Factory control system", in *Proc. PCaPAC2016*, Campinas, Brazil, Oct. 2016, paper WEPOPRP011, pp. 31-34. doi:10.18429/JACoW-PCaPAC2016-WEPOPRP011

[4] A. Uchiyama, M. Komiyama, M. Kidera, and N. Fukunishi, "Data archive system for super conducting RIKEN linear accelerator at RIBF", in *Proc. IPAC2021*, Campinas, Brazil, May 2021, paper TUPAB297, pp. 2178–2181. doi:10.18429/JACoW-IPAC2021-TUPAB297

[5] H. Sakamoto *et al.*, "HIS: The radiation safety interlock system for the RIKEN RI Beam Factory," *RIKEN Accel. Prog. Rep.,* vol. 37, p. 281, 2004.

[6] M. Komiyama, M. Fujimaki, I. Yokoyama, and M. Kase, "Status of control and beam interlock system for RARF and RIBF," *RIKEN Accel. Prog. Rep.*, vol. 39, pp. 239, 2006.

[7] Melsec-Q, https://www.mitsubishielectric.co.jp/fa/products/cnt/plcq/items

[8] FA-M3, http://www.FA-M3.com/jp

[9] FL-net, https://www.iemanet.or.jp/Japanese/standard/open

[10] M. Komiyama *et al.*, "Performance Verification of New Machine Protection System Prototype for RIKEN RI Beam Factory", in *Proc. ICALEPCS'21*, Shanghai, China, Oct. 2021, pp. 742-745. doi:10.18429/JACoW-ICALEPCS2021-WEPV038

[11] Yokogawa Electric corporation, "Catalog of F3DF01-0N", unpublished.

[12] A. Uchiyama *et al.*, "Control System of the SRILAC Project at RIBF", in *Proc. ICALEPCS'21*, Shanghai, China, Oct. 2021, pp. 147-152. doi:10.18429/JACoW-ICALEPCS2021-MOPV015

[13] CompactRIO, https://www.ni.com/ja-jp/shop/compactrio.html

[14] LabVIEW, https://www.ni.com/ja-jp/shop/labview.html

[15] CSS, https://controlsystemstudio.org

[16] COEIROINK, https://coeiroink.com

[17] A. Uchiyama *et al.*, "Development of machine protection system for SRILAC", in *Proc. the 18th Annual Meeting of Particle Accelerator Society of Japan*, online, Aug. 2021, pp. 532-535.