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LCLS-II CONTROL SOFTWARE ARCHITECTURE FOR THE WIRE SCANNER DIAGNOSTICS*

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Abstract

The Super Conducting (SC) Linac Coherent Light Source II (LCLS-II) facility at SLAC is capable of delivering electron beam at a fast rate of up to 1 MHz. The high rate necessitates the processing algorithms and data exchanges with other similar systems to be implemented with FPGA technology. For LCLS-II, SLAC has deployed a common platform solution (hardware, firmware, software) which is used by timing, machine protection and diagnostics systems. The wire scanner diagnostic system uses this solution to acquire beam synchronous time-stamped readings, of wire scanner position and beam loss during the scan, for each individual bunch. This paper explores the software architecture and control system integration for LCLS-II wire scanners using the common platform solution.

INTRODUCTION

For measuring the transverse electron beam profiles and emittance at various locations, wire scanners (Fig. 1) are one of the primary tools installed and commissioned for use at SLAC [1]. There are two flavors of wire scanners – a fast wire scanner and a slow wire scanner. The fast wire scanner system is comprised of a linear motor stage with an incremental linear encoder for closed loop position feedback [2]. The slow wire scanner system is comprised of a stepper motor and a linear Variable Differential Transformer (LVDT) and an incremental encoder on motor shaft for position feedback. On both the styles of wire scanner, the movable stage holds a wire card. The wire card holds thin wires (in the order of 20 nm), generally much smaller than the beam transverse size (which can range from 40 to 300 um) [3].

As this thin wire passes through the electron in the transverse direction, it intercepts the portion of the beam incident on it, creating gamma radiation captured by photodiode detectors. The intensity of these beam loss readings obtained during a scan of the wire card through multiple bunches of the beam, helps provide the cross section of the beam. This measurement depends on several parameters. For e.g.: the thickness of the wire, the repetition rate with which the electron beam is incident on the wire, the speed with which the wire moves to intercept the beam, to name a few.

The higher beam rate of LCLS-II could damage the wires [3, 4]. Thus, for higher repetition rate, the wire needs to move faster through the beam region to prevent damage while still making a reasonable measurement. To prevent this damage, a minimum speed is defined. The wire scanner firmware is required to communicate to the Machine Protection System (MPS) if the minimum speed has not been reached prior to the wire intercepting the beam [4].

For LCLS-II, long radiation-hard optical fibres are installed from the electron gun to the beam dump as part of Beam Containment System. Beam losses generate gamma radiation that travels through the fiber. A photomultiplier tube (PMT) is installed at the end that measures this light. Signal from this PMT is used by the wire scanner.

In this paper, we will detail the software architecture of LCLS-II wire scanner system. We will also briefly describe the system for beam synchronous data acquisition for wire scanner. Wire scanner system also uses common platform solution to implement the MPS requirement and PMT signal readback. Details of this implementation will be provided in this paper.

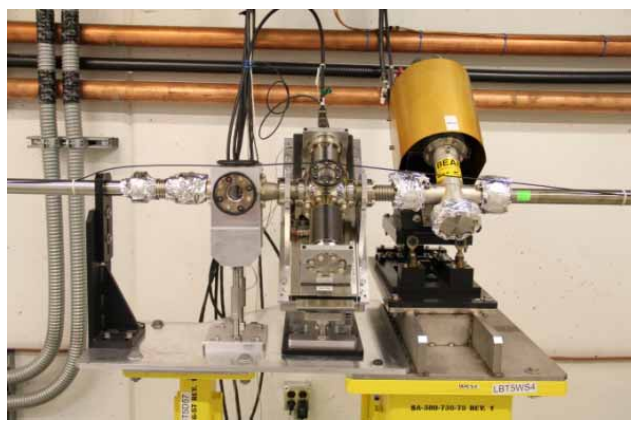

Figure 1: Fast Wire Scanner and a Slow Wire Scanner at SLAC.

CONTROL SYSTEM

Software Architecture Overview

Wire scanner controls is broadly split into 4 different stack system (Fig. 2). At the lowest level, we have the motion controller which is used for trajectory planning and closed loop control. On top of this layer is the wire scanner FPGA which is used to provide the wire position and beam loss signal, beam synchronously, to EPICS. This layer also handles the MPS Fault detection. EPICS IOC layer determines the scan parameters for motion controller and Beam Loss Signal Integration Settings for FPGA. Lastly, client software such High Level Applications or User Interfaces performs the emittance measurement calculations.

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Aerotech Motion Controller.

For LCLS-II, Aerotech Ensemble CP20 drives are used for position feedback control. These drives support 20 A peak current which satisfies the requirements for LinMot linear motor PS01-37x-120F-HP-C20 used for fast wire scanners.

On these Ensemble drives, a user can run up to 5 programs, in AeroBasic programming Language, with configurable parameters for memory allocation. A Task Manager is run continuously as one of the programs. This task receives relevant scan parameters using GLOBAL variables from EPICS. This task manager also defines how the controller must take preventive action in the event of an axis fault or task fault by defining user defined functions [5]. These are invoked by using ONAXISFAULT and ONTASKERROR commands. Recovery actions include homing / retracting the motor to a safe out of beam position and then disabling the axis torque. This is defined in the event of a fault such as motor over-current. As mentioned in the previous section, this is to prevent the motor from halting in the middle of the scan range and potentially damaging the wire.

Unstable motor current oscillations when the servo loop is not optimally tuned has exhibited interference with beam steering and jitter due to stray magnetic field [4]. Ensemble Digital Scope system is heavily utilized for tuning the position feedback loop of the motor. Aerotech's Easy Tune tool from Digital Scope provides easy interface for optimizing servo loop tuning of servo filters and loop gains [5].

A wire scan routine is set up as the second task on the controller. LINEAR motion command with S-curve trajectory definitions is programmed to be used for on-the fly scans. This routine also provides the capability to run the LCLS style step scans.

ATCA Crate

For LCLS-II, real-time position data capture is done through a common platform carrier board with an FPGA on an Advanced Telecommunication Computing Architecture (ATCA) crate [6]. As the ATCA crate is shared between multiple systems, slot 2 on the ATCA crate is reserved for MPS application. MPS carrier board receives timing information and distributes it to other carriers (including wire scanner board) through the back plane. The ATCA back plane's zone 2 interface is used to connect MPS network to all carrier boards for communication [7]

The encoder data is first read in from a rear transition module (RTM). Exclusive-or gates in the circuitry are used for encoder-loss detection. An RS422 transceiver handles re-transmission of encoder signals to the motion controller [8]. An RS422 transceiver handles isolation and conversion of differential encoder signals to single ended signals for FPGA.

MPS Fault Protection Logic

As established previously, the wire scanner must reach a minimum speed before intercepting the beam with its wire card to prevent damage to the wire. The wire scanner must signal the MPS at least 100 us before the wire reaches the beam if the minimum speed has not been reached so that the MPS has time to take preventative action [4, 9]. Wire scanner firmware on FPGA supports the MPS fault protection logic.

A simple diagram defining the inputs to MPS logic is shown in Fig. 2. Limit switch information is obtained from the motion controller and encoder information is obtained from RTM. If the device is on the low limit, MPS logic is ignored, and device is in an OK state. In the event of an encoder fault condition, the speed will be considered 0 and MPS logic will be set to FAULT condition.

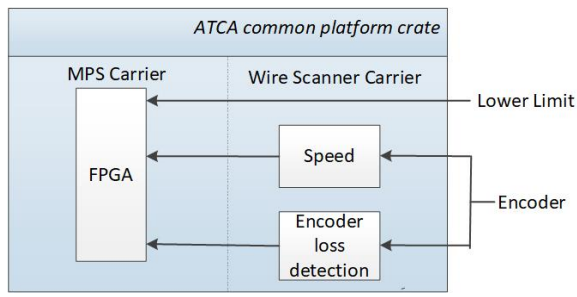

Figure 2: Simple diagram with Inputs to MPS system.

MPS fault detection algorithm uses 4 position thresholds (Fig. 3).

- Lower limit switch position
- Start of region where wire may be present so wire scanner must reach minimum speed.
- End of region of where wire may be present.
- Position where wire scanner will come to a stop to change direction to retract to home/ lower limit.

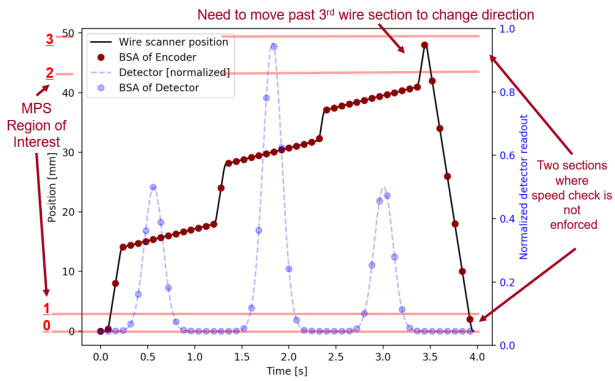

Figure 3: Position thresholds in an example wire scan [8].

In Fig. 3, 0-1 and 2-3 define the two regions of the wire scanner travel range where MPS speed calculation is ignored. In these two regions, the stage will be accelerating/decelerating rapidly to reach the necessary speeds [8]. The logic flow for MPS Fault protection is shown in Fig. 4 The minimum speed or MPS speed calculation (in mm/sec) for a safe wire scan is defined in Eq. (1).

$$v_{mps} = 0.32 * sqrt(2) * 1000 * \frac{f_{rep}}{600000}, \qquad (1)$$

where f_{rep} is the current beam rate. This speed threshold is relayed to the FPGA from EPICS IOC as encoder timeout

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threshold. To calculate the speed in terms of encoder timeout transitions, a few other parameters are to be considered. The minimum step size for the wire is defined as 4 um [4, 8]. Each encoder transition takes 6.4 ns of FPGA clock cycles. So, for v_{mps} (in mm/sec) minimum speed, the timeout threshold is defined in Eq. (2).

$$timeout_{mps} = \frac{v_{mps}}{0.004*6.4*10^9} \quad (2)$$

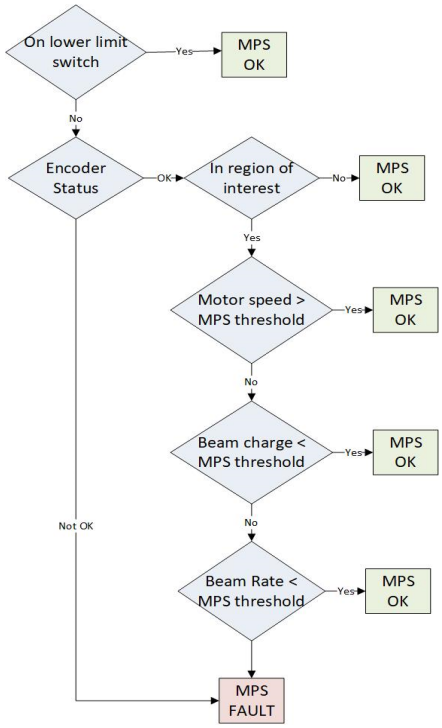

Figure 4: Flow chart depicting Wire Scanner MPS Logic for LCLS-II.

The beam charge and beam rate defined at the beginning of wire scan are saved into 2 threshold registers. These parameters are continuously monitored over the scan process. In the event where the actual beam charge or beam rate differs from the saved threshold value, MPS OK state will be revoked. The current beam charge (as part of bunch information field) and beam rate information is obtained from the timing pattern and read directly into the FPGA as described in the previous section through the ATCA backplane [10].

Digital Integration of Wire scanner Beam Loss Signal

The common platform system allows for the installation of AMC cards (high speed- digitizers) which can provide application-specific functionality to interface with the FPGA. The wire scanner system utilizes one of these standard AMC cards that provides 3 channels of 350 Ms/s 16-bit ADC card. Through this ADC channel beam loss monitor signal is read into the system.

For detection of loss from wire passing through the beam, wire scanner system utilizes the diagnostic output from BCS LBLM chassis. An external amplifier with adjustable gain is added to facilitate visualization of losses from a wire (Fig. 5). The fast diagnostic waveform showing the arrival time of a loss pulse at the Photo Multiplier Tube is used for loss detection. An example loss signal is shown in Fig. 6.

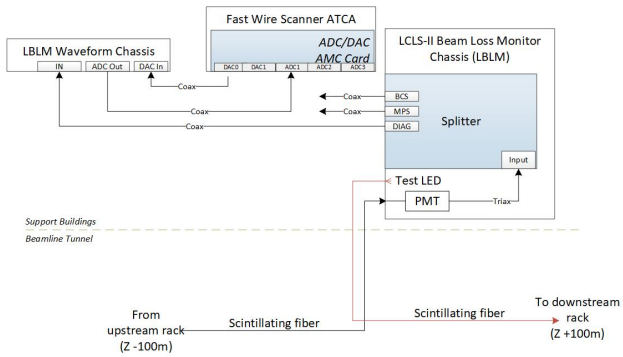

Figure 5: Wire scanner Loss Monitor Schematic.

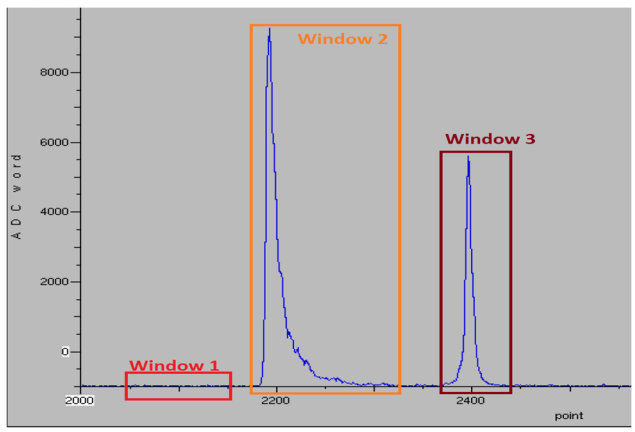

Figure 6: Example beam loss signal waveform marked with integration windows [LCLS Physics Log Entry, 2017/12/06].

Numerical integration over these peaks gives the charge scattered by the wire. Integration algorithm focuses on the windows as shown in the Fig. 6. The three areas of integration have their own trigger settings for window start and window width. Window 1 defines the pedestal region. This defines the background reading as seen by the ADC. Window 2 selects the region where beam loss from wire scan can be seen. This region is also known as the gated region. Window 3 or offset is for adjusting non-normalized sums (unused currently). Result is reported as difference between the gated region and the pedestal region. To define the linear integration equation, each window has an added flexibility to define separate coefficients A_0 and A_1. These coefficients can be used to compensate for the difference in number of samples in the pedestal vs the gated region. Thus, the integration equation is defined in Eq. (3).

$$A = A_1 * Sum_{gate} - A_0 * Sum_{pedestal} + Offset \quad (3)$$

During commissioning of wire scanners, a graphical user interface (GUI) using the Python Display Manager (PyDM) was used to display the diagnostic waveform. Integration gate for wire scans were identified from the waveform display (Fig. 7). Once the integration windows

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are set, plotting the result from the gated integral over wire scanner position shows the loss from the wires. Figure 8 shows result from scanning wire scanner WSBP2 on detector LBLMBPN15.

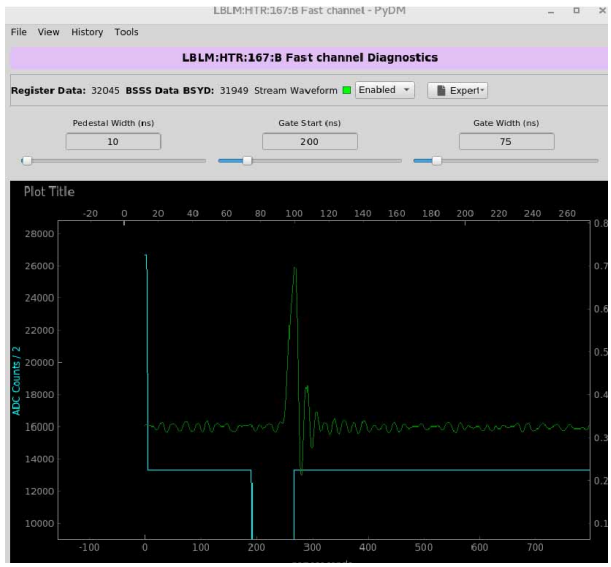

Figure 7: PyDM GUI used for identifying integration windows.

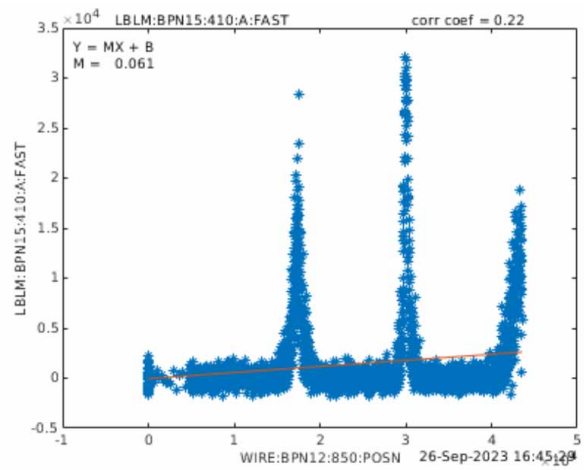

Figure 8: Wire scan of WSBP2 as seen from at the detector [LCLS-II Physics Log Entry, 2023/09/26].

Based on a known loss point and the propagation speed, the peak on the diagnostic waveform can also be used to define the location of loss along the beam path.

$$z = t * \frac{c}{n-1} * 10^{-9} + t_{ref} * \frac{c}{1-n} + z_{ref} . \quad (4)$$

In Eq. (4) z defines the location of the loss based on arrival time t. c is the speed of light and n is the refractive index of the fiber. z_{ref} and t_{ref} are known loss location and point in time respectively [11].

CONCLUSION

The LCLS-II wire scanner system heavily leverages the services of the SLAC common platform to implement high-speed position acquisition and to interact with other high-performance system like MPS. 20 wire scanners have been deployed with this controls infrastructure. The control system for LCLS-II Fast Wire scanner system has been used successfully during commissioning of SC beam up to the Hard X-ray and Soft X-ray undulator line.

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