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LANSCE's TIMING SYSTEM STATUS AND FUTURE PLANS*

L. E. Walker†, B. C. Atencio, S. A. Baily, D. Fratantonio, C. D. Hatch, M. Pieck, T. Ramakrishnan, Los Alamos National Laboratory, Los Alamos, NM 87545, USA

Abstract

The Los Alamos Neutron Science Center (LANSCE) operates at a maximum repetition rate of 120 Hz. Timing gates are required for synchronization of the accelerator to provide beam acceleration along the LINAC and beam distribution to the five experimental areas. They are also provided to other devices with sensitive operating points relative to the machine cycle. Over the last 50 years of operations many new time sensitive pieces of equipment have been added. This has changed the demand on, and complexity of, the timing system. Further driven by equipment obsolescence issues, the timing system underwent many upgrades and revitalization efforts, with the most significant deployment starting in 2016. Due to these upgrade efforts, the timing system architecture design changed from a purely centralized system, to a distributed event-based one. The purpose of this paper is to detail the current state of the timing system, as a hybrid system with the gate events being generated from a new timing master system, while still utilizing legacy distribution and fanout systems. Upgrades to the distribution system are planned, but due to the required beam delivery schedule, they can only be deployed in sections during four-month annual maintenance cycles. The paper will also cover the off-the-shelf solutions that have been found for standardization, and the efforts towards a life cycle management process.

INTRODUCTION

When the timing system was first deployed at the site currently known as Los Alamos Neutron Science Center (LANSCE) it was state of the art. However, that deployment was several decades ago and with any facility that has been running for a long time, the timing system is in need of an upgrade. Since the construction of LANSCE more user facilities have been added to create a total of five that are currently in use today. The timing system can produce 120 Hz timing signals, which is then divided between the five user facilities. This is done by scheduling a flavor gate with definable repetition rates and lengths for each user facility. In addition to sending beam to more users, there is an added complexity that each user facility requires their own independently timed equipment, such as fast kicking magnets, beam diagnostics, current monitors, and spill detectors requiring a variety of interacting timing signals.

The timing system at LANSCE consists of several generations of both commercial off the shelf (COTS) and custom-made components that require significant effort to maintain. A timing system modernization effort began with its conceptualization in 2007 and deployment in 2016 [1, 2].

† lwalker@lanl.gov

Within the last seven years, approximately 120 new timing Input/Output Controllers (IOCs) have been deployed throughout the facility. Great progress has been made, but there are still upgrades needed that will expand the facilities capabilities and allow the site to operate for years to come.

CURRENT SYSTEM DESCRIPTION

Changing technologies throughout LANSCE's years of operation have led to many variations in the hardware deployed for the timing system. In 2016, the facility began an upgrade from CAMAC crates with a MicroVAX computer controller to a new timing system designed around the Micro Research Finland (MRF) timing event system [3, 4]. The MRF timing modules are available off the shelf and provide the features that are needed for the diverse timing system at LANSCE. The MRF event generators (EVGs) and event receivers (EVRs) work together to create the event-based timing structure. This upgrade is still ongoing, leaving the timing system in a hybrid state.

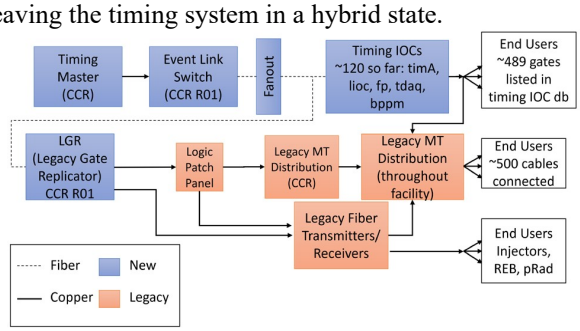

Figure 1: Hybrid state of timing system.

Figure 1 shows the current status of the timing system. The timing master, event link switch, fanout, and timing IOCs have been upgraded and deployed. The Legacy Gate Replicator (LGR) was installed to reproduce the 96 gates that were formed by the old timing system for distribution. This leaves the Logic Patch Panel, Legacy Master Timer Distribution, legacy Fiber Transmitters/Receivers systems to redesign and deploy.

Timing Master

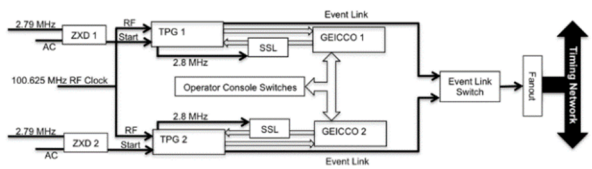

Figure 2: Timing Master System.

The Timing Master uses a redundant scheme, with the second system running in hot-swappable standby configuration in the event there is a failure in the primary

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controller. Figure 2 shows the communication between the modules and the Timing Master [2].

The Zero-Crossing Detector's (ZXD's) purpose is to monitor the facility AC line crossing and provide a 120 Hz trigger to the Timing Pattern Generator (TPG) so that each machine cycle can be timed such that RF stations are turned on during the peak of the AC cycle [5].

The TPG is used to synchronize and distribute the scheduled timing solution to the timing IOCs. The output has less jitter than one cycle of the reference clock signal, or 9.9 ns. The TPG crate will also output the cycle-by-cycle flavor map for the specific event sequence.

The Slave Synchronization Logic board (SSL) is built as a VME rear transition module. The purpose of the SSL is to ensure that all the enabled slave event generators inside of the TPG start the gate pulses at the same time.

A set of Gate Enable, Inhibit, and Countdown Controllers (GEICCOs) were also installed to enable and disable gate signals dependent on the enable/disable switches controlled by the operators, as well as the delivery mode (i.e., single shot, multi-shot mode, continuous "burst" mode, continuous "burst of bursts" mode, cycle stealing mode, and asynchronous mode). The GEICCO also provides a timeout feature, where if the "Cycle-End" gate is not received within 3 milliseconds of the scheduled time, the TPG will be considered broken, and the system will switch to the other TPG and GEICCO pair.

Event Distribution

The timing system utilizes a MRF Fanout Concentrator Module, which is referred to as the Fanout, to switch between the signals of the TPGs with minimal disruption in the event of an issue. This module is used to merge the two TPG signals together and send one buffered output to an uplink, which is sent to another fanout chassis.

After going through these modules, the signal is transmitted over fiber to the EVRs in the field. The fiber distribution is done through the MRF Fanout cards and through a fiber distribution chassis located directly below the crate. This distribution can be done over the same fiber backbone that is used for the rest of the control system network.

Timing IOCs

Once the signal is transmitted over the fiber, the signal is sent to Event Receivers in the field. The local event receivers for dedicated timing IOCs are housed in CompactPCI crates with an embedded controller from Abaco, the CR-12 [6]. The CR-12 programs the EVR with the gates that it needs to output. These gates come from the universal output connectors on the front of the EVR. LEMO cables are connected to the front panel and fed to a patch panel where the equipment can then be connected directly, or the signal can be connected to the legacy distribution chassis.

EVRs have also been deployed in systems not dedicated solely for accelerator timing. The Timed and Flavored Data Acquisition (TDAQ) and the Beam Position and Phase Monitor (BPPM) crates contain an EVR that provides cycle start for the data acquisition modules to provide the timing and flavoring aspect of the data collection. These signals are provided internally in the crate. The crates have the capability of containing a combination of four TDAQs or BPPMs. This leaves an availability of eight spare timing channels. The extra gate outputs are connected to a patch panel and can be used to provide gates to other equipment.

There have been upgrades throughout the site to provide fast protect systems with the necessary timing gates generated from EVRs. Additionally, EVRs have been deployed by the low-level RF team to provide gates to the RF amplifiers that can be switched on a cycle-by-cyle basis to delayed or normal timing. This enables mulit-energy mode beam delivery, where one species can be delivered at 800MeV, while a second species can be delivered at a lower energy.

Legacy Gate Distribution

Some gates are connected to equipment directly from the 3.3V EVR output ports, but most timing gates are still distributed though the 15V legacy distribution chassis. Legacy timing distribution chassis are located throughout the facility. Their purpose is twofold: provide line driving capability to drive the often-half-mile long 50-ohm coax timing distribution cables, as well as to serve as local fanouts to distribute signals to end-user equipment.

Logic Patch Panel

The MRF event-based system is not able to create a timing gate that is a combination of signals if there is a chance they will overlap, creating the need for the Logic Patch Panel. The patch panel uses a combination of AND gates, OR gates, invertors, and flip flops to make these combination gates.

FUTURE UPGRADES

Legacy Gate Distribution

The parts on the line driver cards for the legacy distribution units have become difficult to acquire. Additionally, replacing the custom hardware with commercial off the shelf parts will make the spares more readily available and increase the longevity of the controls system. The current legacy chassis consists of 8 1x4 fanouts which accepts either 5 or 15 V input signals and distributes transformer-coupled 15 V outputs. There is currently a commercial off the shelf replacement, manufactured by Meinburg, being tested for the distribution portion of the chassis [7]. The unit will take two input signals and produces 24 output signals on a 1x12 basis. The output is 2.5 V at 50 Ohms. The output signal delay will be less than 24 nanoseconds. The chassis comes in a 1U form factor and has the advantage of containing an LED that illuminates when a gate is present at the input. For these pieces of equipment that need the 15 V signal present, there will need to be level converters added until the legacy equipment is upgraded by the equipment owners. The amplifier is still in the design phase and will need to be prototyped before it is deployed.

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Logic Patch Panel

The Logic Patch Panel in the Central Control Room also needs to be redesigned to update the system. The intention is to distribute local logic gate units in the field beside the event receivers. The team has purchased a programmable logic unit manufactured by Caen to test the feasibility of use in the facility [8].

Timing IOC Processors

Currently the timing IOCs use a CR-12 module as the processor. The CR-12 is a 6U Compact CPI single board computer. It has an Intel Core i7 processor with up to 8 GB of memory. The CR-12 module has been retired from production and we currently do not have a method to obtain spares. The search for the replacement is still in progress.

STANDARIZATION

At the beginning of the timing system upgrade, the idea was to standardize the system by deploying identical hardware with the same outputs programmed. However, this was soon determined to be unreasonable given the substantial number of EVRs and the non-uniformity in assigning EVR output gates. Due to the varying requirements of each location, custom EVR gate loadouts with varying numbers of duplicates have to be deployed. Some areas required more gates than the twelve-output capacity of a single EVR and therefore needed multiple EVRs to generate all the signals required. An additional deviation from a completely standardized timing distribution system is that multiple form factors are used for timing IOCs. In addition to the CR-12 SBCs, rootport modules in the TDAQ/BPPM crates are used as timing IOCs. The ability to utilize multiple form factors for timing IOCs is a benefit of the EPICs and timing system architecture in that it provides long-term upgrade paths, but also comes with the challenges associated with maintaining multiple timing IOC hardware form factors.

The first step taken to standardize the system was to standardize the EVR board hardware. The EVRs have all been configured to be identical with universal I/O TTL modules installed on the cards. Every card has all twelve modules installed, even if there is no current intention of utilizing each output. This will allow for gates to be easily added in the future, since all the hardware is installed, and it will only require a software change to send the gate to the appropriate output. Additionally, each location that has an EVR deployed also has a breakout BNC panel installed. This allows for easy connection for the external equipment.

Another step that was taken to normalize the timing system was to standardize the outputs wherever possible. An example of this is the TDAQ and BPPM systems. The crate will contain at least one module that needs the cycle start, the module in the first slot of the chassis. There is a possibility of the crate containing three other modules that will require the same gate. Therefore channel 0, 9, 10, and 11 on these systems are reserved for internal crate use. The output is only programmed when the gate is needed, but they are not connected to the rear breakout panel and cannot be connected to other equipment.

DOCUMENTATION

Another challenge is not knowing what equipment is still using the timing gates provided. There is some documentation of the legacy distribution chassis and the output gates, but it is out of date. Many of the system changes were not updated in the documentation. Some of the descriptions listed in the termination field on the documentation needed additional details as well. Several of the entries are simply listed as a rack location and does not contain the device name. A multi-team effort has been made to update the documentation of the existing system and record what each of the gates are connected to.

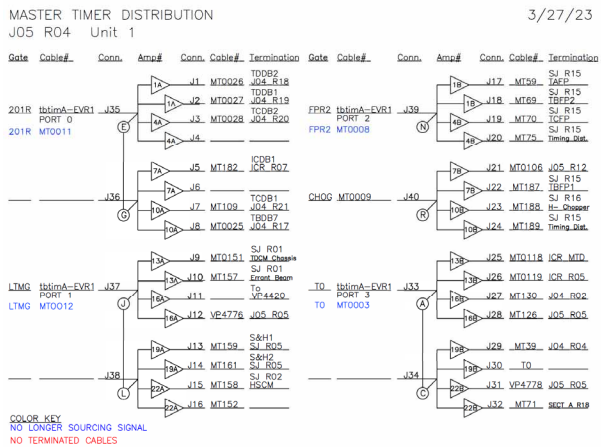

Figure 3: Documentation for Legacy Unit.

An example of the Legacy Distribution Unit Documentation can be seen in Fig. 3. To ensure the documentation is up to date, we began by confirming which cables were still connected to the legacy distribution units. This was done by performing a visual inspection of the chassis in the field. Any outputs that have been removed were annotated in the documentation and will be deleted. The next step is to trace out the other end of the cable to see what equipment the cable goes to. After the end point information is gathered, the equipment will be verified to see if it is still operating and if it still needs the gate. This effort is still ongoing and is expected to be completed during the upcoming maintenance cycle.

The same effort is being made to trace out the cables that are sourced from the EVRs in the field. Additionally, there has been coordination with the Controls Software Team to develop a better documentation method. The main benefit to the new program is that a lot of the information is auto generated from database files of deployed timing IOCs. This will lead to less human error in the documentation and ensures that the displayed documentation accurately reflects the current operational state of each system. Figure 4 is an example of the output of this program. The field of EVR Port# is auto populated and consistent throughout the documentation for each EVR. The Gate field is also auto populated to display the name of the gate that is programmed to be sent out the universal output of the EVR

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module. In some cases, the name of the equipment will also be filled in automatically.

However, in most cases, the rack and equipment will need to be manually entered. This information will be provided to the software team when requesting a new output to allow for seamless entry of the data. The other advantage to the new documentation program is that the information will update in real time. As soon as an output is programmed, it will update the documentation with the name of that gate.

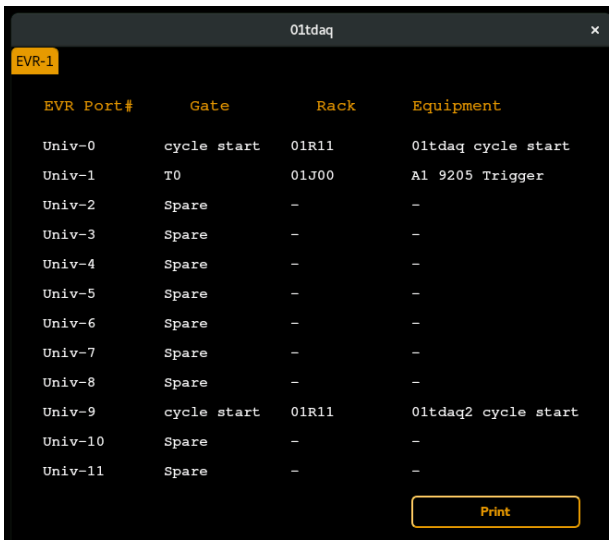

Figure 4: EVR Documentation.

This documentation effort is important to determine the best path forward for the timing system and streamline the deployment process. There have been several gates found that are no longer utilized and therefore no longer have to be generated. This could potentially minimize the number of EVRs and programmable logic units that will need to be deployed.

LIFE CYCLE MANAGEMENT

Commercial off the shelf equipment is being used wherever possible. This will prevent future generations being left in the same predicament of having an unmanageable timing system with custom made equipment and no ability to maintain it. The steps taken to standardize the system will also make it easier to maintain.

Care will also need to be taken to account for the production cycle of the modules. Some of the modules that are currently used in our system, such as the CR-12, are no longer being manufactured. With the discovery that some of the spare modules are no longer viable, the spare inventory is dangerously low. Once an upgrade path is determined, the modules will have to start being replaced.

SUMMARY

The timing system is more distributed than the legacy, solely centralized, system. However, the timing system can never be completely distributed, as the clock will need to come from one common source. The gate signals that are sent to the accelerator equipment are generated locally from an event structure. Distributing the timing gates means that fewer cables will need to be pulled. The new timing upgrades will allow for more timing gates to be generated, whereas the old timing system was limited to 96 gates. The distributed system is not even limited by the number of events that it can generate, as now only the trigger, length, and delay need to be set up and sent to the EVR. Other benefits of this new system include better resolution, precision, and less jitter.

The benefits of the documentation have already been seen. Having a thorough understanding where signals are sourced from, and the equipment that it connects to, makes a system easier to maintain and troubleshoot when a problem arises. Removing the dependency on legacy equipment will do the same.

The timing system upgrade has been an ongoing, multi-year process. There are still a lot of decisions that need to be made to finish upgrading the timing system. The current efforts in documentation and standardization will provide the required information to make the necessary decisions.

ACKNOWLEDGEMENT

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