ISBN: 978-3-95450-238-7 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS2023-THPDP056

CONSOLIDATION OF THE POWER TRIGGER CONTROLLERS OF THE LHC BEAM DUMPING SYSTEM

L. Strobino*, N. Magnin, N. Voumard, CERN, Geneva, Switzerland

Abstract

The Power Trigger Controller (PTC) of the LHC Beam Dumping System (LBDS) is in charge of the control and supervision of the Power Trigger Units (PTU), which are used to trigger the conduction of the 50 High-Voltage Pulsed Generators (HVPG) of the LBDS kicker magnets. This card is integrated in an Industrial Control System (ICS) and has the double role of controlling the PTU operating mode and monitoring its status, and of supervising the LBDS triggering and re-triggering systems.

As part of the LBDS consolidation during the LHC Long Shutdown 2 (LS2), a new PTC card was designed, based on a System-on-Chip (SoC) implemented in an FPGA. The FPGA contains an ARM Cortex-M3 softcore processor and all the required peripherals to communicate with onboard ADCs and DACs (3rd-party IPs or custom-made ones) as well as with an interchangeable fieldbus communication module, allowing the board to be integrated in various types of industrial control networks in view of future evolution.

This new architecture is presented together with the advantages in terms of modularity and reusability for future projects.

INTRODUCTION

LHC Beam Dumping System

The LHC Beam Dumping System (LBDS) is a critical system ensuring safe extraction of the beams from the LHC. Each counter-rotating beam is sent to its extraction channel using 15 extraction kicker magnets (MKD) and 15 extraction septa (MSD). It is then diluted by 4 horizontal (MKBH) and 6 vertical (MKBV) dilution magnets on the beam dump absorber (TDE). To allow for the rising edge of the MKD magnetic field, a particle-free Beam Abort Gap (BAG) of 3 µs is maintained in LHC [1].

Dump Requests (DR) come from 3 different sources: the machine protection system for emergencies, the machine timing system for scheduled dumps, or the LBDS itself in case of internal failures. These spontaneously issued dump requests are synchronized with the BAG by the Trigger Synchronization Units (TSU). Synchronous dump triggers are then distributed through the Trigger Fan-Out units (TFO) to the High-Voltage Pulsed Generators (HVPG) [2].

50 HVPGs power the MKDs and MKBs. At the reception of a trigger, two redundant Power Trigger Units (PTU), each comprising a Power Trigger Controller (PTC) and two redundant Power Trigger Modules (PTM), start the conduction of two switches composed of Fast High Current Thyristors (FHCT) that discharge capacitors into the magnet. In addition, a redundant fault-tolerant Re-Triggering System (RTS) allows the asynchronous fast re-trigger of all HVPGs if one HVPG self-triggers. Each HVPG is equipped with two Re-Trigger Boxes (RTB), that couple internal pickup signals to the redundant Re-Trigger Lines (RTL) to generate a pulse when the HVPG is triggered, and also capture the pulses on the RTLs and send them to their PTUs.

Figure 1 shows a simplified schematics of the redundant trigger distribution from the TSUs and the RTBs to the PTUs.

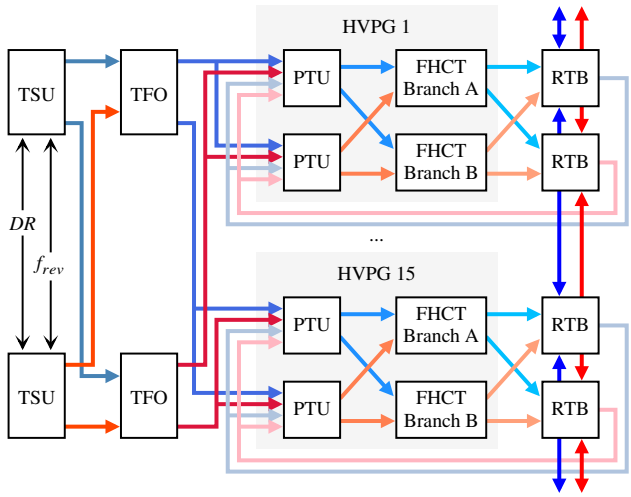

Figure 1: LBDS trigger distribution architecture.

Power Trigger Units

A PTU is composed of several internal low and high-voltage power supplies, two PTMs operated in parallel, and one PTC to control, monitor, and interlock the PTU. All modules are connected together through a backplane, as shown in Fig. 2. Each PTU has 5 trigger inputs: two for synchronous triggers from two redundant TFOs, two for asynchronous triggers coming from the RTLs through redundant RTBs, and one software trigger input, used for test purposes. The PTU also receives a copy of the signals present at the input of one of the RTB, to be monitored by the PTC (no redundancy here: each PTU monitors one RTB).

The PTMs comprise a principal circuit generating a main trigger pulse of about 800 A for 1 µs, and a compensation circuit maintaining a 50 A average current for a duration of about 400 µs [3]. The principal circuit is powered from a +4 kV power supply and is controlled by 3 series-connected high-voltage IGBTs, triggered through pulse transformers by a gate driver circuit operating from a +48 V power supply. For added redundancy, each PTM is connected to a different FHCT (branches A and B in Fig. 1), in parallel with a second PTM from the other PTU.

* lea.strobino@cern.ch

ISBN: 978-3-95450-238-7 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS2023-THPDP056

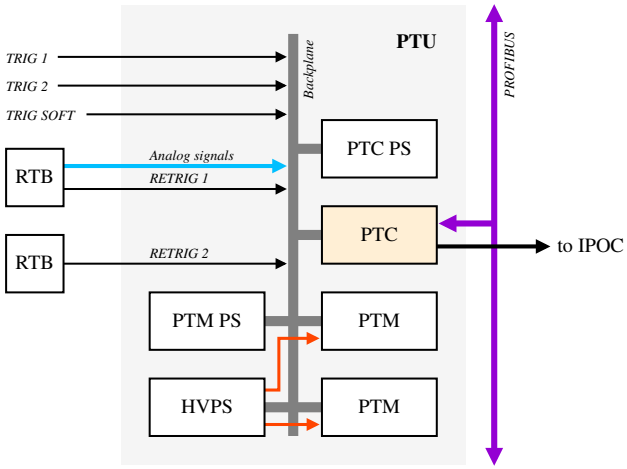

Figure 2: Block diagram of a PTU, comprising two PTMs, a PTC, and several low and high-voltage power supplies.

Power Trigger Controller

The PTC has the double role of controlling the PTU operating mode and monitoring its status, and of supervising the LBDS triggering and re-triggering systems.

It controls the +4 kV power supply of the PTMs and continuously monitors its voltage from a dedicated divider, located at the output of the power supply, and also indirectly from dividers inside the PTMs, connected to one of the 3 series IGBTs. This allows to check the voltage sharing between the 3 IGBTs, which should be similar if their leakage current is the same, and also to detect if one of the IGBTs is in short-circuit. Additionally, the PTC monitors the rest of the PTMs power supplies with window comparators.

When the PTC detects one of the 5 triggers on the backplane, it performs a post-mortem analysis of the PTU and the RTB. In particular, it checks that the two synchronous triggers were received first and, as a consequence of the HVPG pulsing, that the two asynchronous triggers were received afterwards, within a given time window. It then checks that the PTMs principal and compensation currents were nominal, and that the PTMs gate driver circuits stayed active for the expected duration. Finally, it makes sure that the 5 pickup signals at the input of the RTB were received.

The results of the continuous monitoring and the post-mortem analyses are sent to the industrial control system of the LBDS, namely the State Control and Surveillance System (SCSS), through a fieldbus. A faulty status either makes the SCSS issue a dump request to the TSUs in case of continuous monitoring, or prevents rearming the LBDS in case of post-mortem analysis.

Additionally, upon receiving a command from the SCSS, the PTC can route the software trigger signal to one of the PTMs, or to any of the inputs or outputs of the RTB. This functionality is used to test the LBDS in local mode, for instance to trigger a single HVPG individually, or to test the RTBs and other analysis systems connected downstream, such as the Internal Post Operation Check (IPOC) and the Spark Activity Monitoring (SAM) systems [4, 5].

DESIGN

As part of the consolidation during the LHC Long Shutdown 2 (LS2), several components of the LBDS were upgraded, which required to design a new PTC:

- New trigger transformers inside the HVPGs [6];
- New PTMs with higher output current, different gate driver circuit, and additional voltage divider connected to one of the IGBTs [3];
- New RTBs with increased voltage on the RTL [7];
- Extension of the IPOC system to analyze the RTB signals for each generator [7];
- Foreseen upgrade of the SCSS fieldbus in the near future.

The new PTC card is presented in Fig. 3. As only the PTMs and the PTC were being upgraded, it was necessary to maintain compatibility with the existing PTU crate (see Fig. 2), both in terms of its form-factor and its connections to the backplane, as it was decided not to redesign the latter.

From previous experience [8], it was chosen to design the PTC as a System-on-Chip (SoC). This consists in a softcore processor, integrated with all the required peripherals, and implemented in an FPGA. The peripherals can either be 3rd-party IPs (e.g. provided by the FPGA manufacturer), custom-made ones tailored to the needs, or generic ones made at CERN and reused in other projects.

Also from past experience [9], it was decided to embed a fieldbus module from HMS Networks. The Anybus CompactCom M40 was selected for its extensive flexibility. These modules are fitted from the front panel of the cards via a CompactFlash type connector, and can easily be replaced to convert the board to a different fieldbus, saving the costs of a new hardware design.

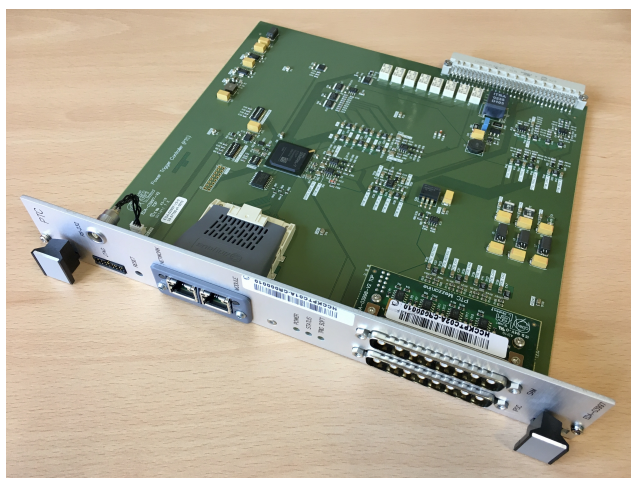

Figure 3: Power Trigger Controller card.

ISBN: 978-3-95450-238-7 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS2023-THPDP056

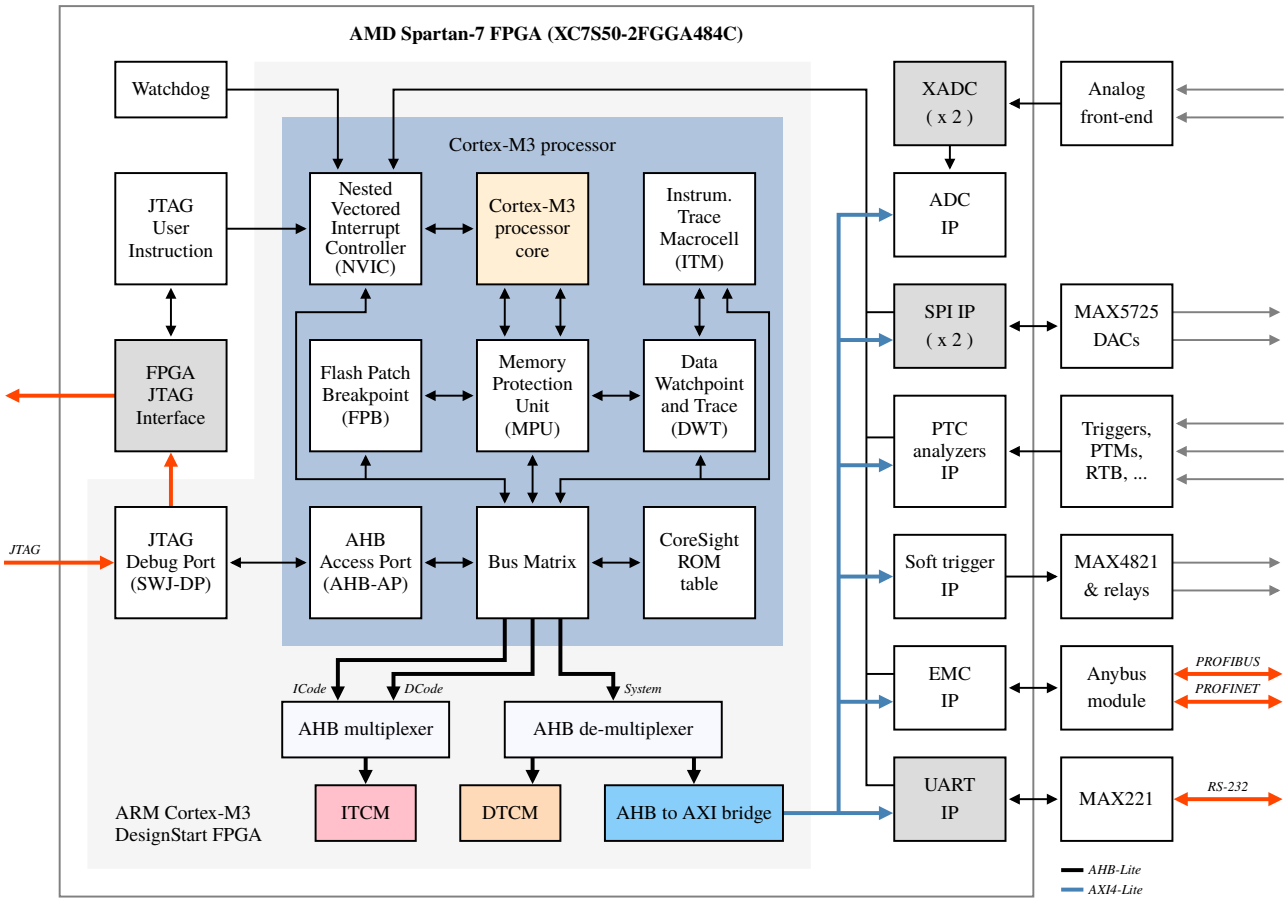

Figure 4: Block diagram of the SoC design of the PTC, implemented in a Spartan-7 FPGA.

System-on-Chip

The SoC is implemented in an AMD Spartan-7 FPGA (XC7S50-2FGGA484C). A block diagram is presented in Fig. 4. The processor and its internal components are shown in the central blue box; their integration in the FPGA environment is comprised in the light gray box. Connected to the AXI bus are several peripherals, either hard IPs (available in the FPGA) or provided by AMD (gray boxes), or custom-made ones written in VHDL (white boxes).

Processor Shortly after the beginning of the project, the ARM Cortex-M3 processor was made available to AMD FPGA users, without any license fees for prototyping, research, and commercial use [10]. This 32-bit processor is targeted at highly deterministic control applications, and offers a very short interrupt latency and an exceptional code density, thanks to the ARM Thumb instruction set. It comes as obfuscated Verilog code, pre-integrated with several components to make it easier to use in an FPGA flow, such as Instruction and Data Tightly Coupled Memories (ITCM and DTCM), made from FPGA block RAMs, and two AHB to AXI bridges.

The Instruction Code (ICode) and Data Code (DCode) AHB interfaces from the processor are combined internally and connected to the ITCM.

The System AHB interface is used to access the DTCM. Any access which is not within the range of the configured DTCM size is presented on the System AXI interface. Since burst transactions and exclusive accesses are incompatible between AHB and AXI buses (exclusive accesses were not part of the original AHB specification), and because the Cortex-M3 converts unaligned accesses on AHB buses to multiple aligned accesses, the AXI bus is restricted to a subset which is directly compatible with AXI4-Lite.

PTC Analyzers Most of the signals analyzed by the PTC during post-mortem analysis are checked by fast comparators (Linear Technology LT1715) with configurable reference voltages. A dedicated gateware IP records these signals at given times after the initial trigger, or records at what time a rising or falling edge occurred.

ADCs The AMD 7-series FPGAs comprise two 12-bit 1 MSPS Analog to Digital Converters (ADCs), which can acquire signals from 17 external analog inputs and from internal sensors. The PTC board includes analog front-ends for filtering and buffering the input signals, which are then connected to the Xilinx ADC (XADC) hard IP inputs. One XADC is dedicated to internal sensors monitoring, such as the core power supplies and the chip temperature. The second one samples 3 analog inputs continuously. A custom-

ISBN: 978-3-95450-238-7 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS2023-THPDP056

made gateware IP monitors the state of the ADCs, reads the data samples as soon as they are available, and keeps them available in registers.

DACs The PTC incorporates 3 Maxim MAX5725 8-channel Digital to Analog Converters (DACs), one for the PTU high-voltage power supply reference, and the other two for voltage references used by the onboard comparators. The processor communicates with the DACs trough two AXI Quad SPI LogiCORE IPs from Xilinx. Each written value is immediately read back, and a faulty state is reported to the SCSS if a discrepancy is detected.

Anybus Module The Anybus CompactCom M40 network module offers several interfaces (16- or 8-bit parallel bus, synchronous serial bus, shift registers), but the full functionality set is only available through the parallel bus. This interface is asynchronous and requires precise timings. An External Memory Controller (EMC) IP was designed to communicate with the module using its 16-bit memory bus, thus making the whole memory space of the module directly accessible from an AXI manager.

Embedded Software

The embedded software was written in C and is responsible for checking the continuously analyzed thresholds, for performing the post-mortem analysis of the data collected by the analyzers IPs, and for the network communication, using software libraries provided by HMS.

Code Memory & RAM The embedded software is stored in the ITCM and is executed from there directly, as this is much faster than executing from the flash memory. A script ran at the end of the gateware implementation writes down which FPGA block RAM corresponds to which part of the memory, then, using IDE tools, the software binary image is split into blocks and placed in the FPGA bitstream, without the need to run the implementation again.

This combined bitstream, containing both the gateware and the software parts, is then written in the PTC flash memory. The embedded software is thus available right after the FPGA configuration, without requiring any bootloader. The ITCM is made read-only thanks to the Memory Protection Unit (MPU) of the processor. The DTCM (i.e. the processor RAM) could have been initialized the same way, but it was chosen to keep the classical approach, where the C library startup code copies the initial RAM content from the load region (in the ITCM) to the execution region, in order to allow software resets.

Network The PTC is currently integrated in the LBDS SCSS using a PROFIBUS fieldbus, however an upgrade to PROFINET is foreseen in the near future. Both networks are already included in the embedded software and were tested in the lab. Except for the network initialization functions and the data endianness, which are network-specific, the network data exchange functions are transparent. The data flow is interrupt-driven in the direction PROFIBUS manager to PTC, and timer-based in the other direction. The PROFIBUS and PROFINET modules can be seen in Fig. 5.

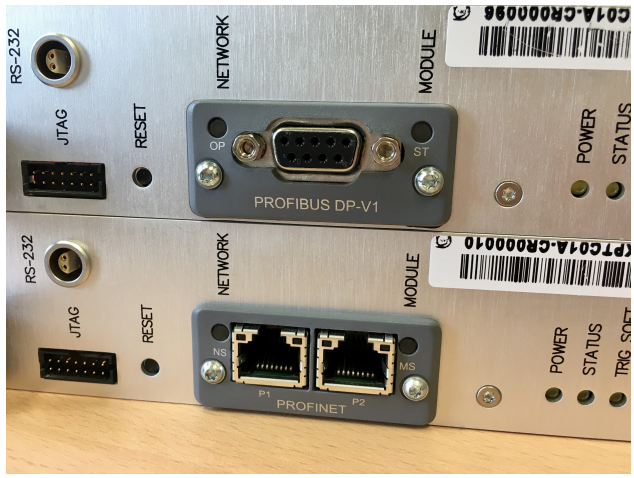

Figure 5: Two PTC cards with different network modules installed, e.g. PROFIBUS (top) and PROFINET (bottom).

Watchdogs & Protection The PTC embedded software is protected by 3 different watchdogs, listed below by increasing timeout (but decreasing diagnostic data).

A basic one is implemented between the SCSS and the PTC using a single bit of the data frame in both directions. The SCSS reads the bit it received from the PTC, flips it, and sends it back, while the PTC reads the bit and sends it back unchanged. The toggling frequency is dictated by the network cycle time (much longer than the PTC cycle time). The SCSS raises an interlock if this frequency drops below a given threshold. A second watchdog is integrated in the Anybus module. If the buffer containing the data to be sent to the SCSS hasn't been updated by the PTC after a given timeout, the module ceases all network participation. This raises all the PTC interlock bits at once in the SCSS. Finally, a third watchdog is included in the PTC gateware. If the embedded software hasn't read the PTC status register after a given timeout, the processor is reset, and with it the network communication.

Additionally, the PTC card monitors its onboard voltages, the communication with the external chips such as the DACs, and the FPGA readback Cyclic Redundancy Check (CRC), aimed at detecting Single Event Upsets (SEUs) causing a configuration memory bit to flip. These statuses are reported to the SCSS.

COMMISSIONING

80 PTC boards were installed in the LHC tunnel caverns (UA63 and UA67) in August 2020. The communication with the SCSS was checked and the cards behaved as expected. The analyzers thresholds were adjusted for the operational conditions in the tunnel, sometimes a bit different than the lab conditions, in particular in terms of grounding. An example of this calibration is given in Fig. 6.

ISBN: 978-3-95450-238-7 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS2023-THPDP056

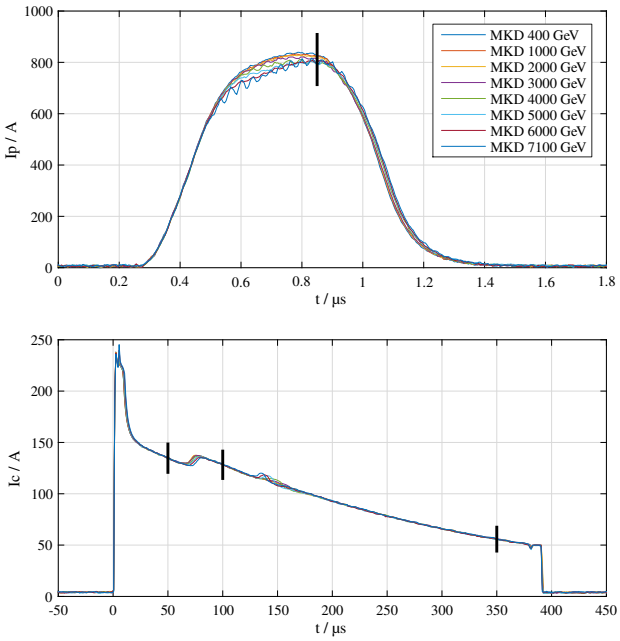

Figure 6: PTC analyzers calibration for the PTM currents, principal (top) and compensation circuits (bottom). The bars are the upper and lower thresholds checked by the PTC.

A few months later, when conditioning the kicker magnets, several PTCs failed with the same signature: the operational amplifiers on the RTB signals (Texas Instruments LM6172), used as analog front-ends but also as line drivers for the signals connected to IPOC, started to oscillate for several hours and then failed. This issue only affected certain boards, but when a board was affected, all its operational amplifiers were affected the same. After trying to reproduce this failure mode in the lab, it was hypothesized that a high-amplitude and high-frequency noise was coupled to the RTB signals, when the HVPGs were pulsing close to their maximum voltage (higher than the bandwidth of the operational amplifiers, so not entirely visible in the acquisition system). Since the operational amplifiers were configured as unity gain buffers and they have a limited, although very high, slew rate, this noise was enough to exceed the maximum differential input voltage of the amplifiers. All the PTCs were then removed from the operational installation to mount an additional passive filter on these inputs, which fortunately had been included in the hardware design as not-mounted components. The issue was solved, and the magnets conditioning could continue.

Finally, during the first half of 2022, a few false-positive interlocks on RTB signals occurred, for some HVPGs only. It was found that a spurious noise was sometimes present at the exact time the PTC was reading the signals. To make the analysis more robust, an improved gateware module was designed, which acquires more points and applies a two-out-of-three logic. This new gateware was successfully tested on two generators until the end of the year, when all the PTC cards were updated.

CONCLUSION

As part of the LBDS consolidation, a new PTC card was designed, based on a modern System-on-Chip architecture, and incorporating an exchangeable network module. This board was commissioned before the start of the LHC Run 3 and performs very well after a few adjustments. Furthermore, it will stay compatible with a potential future upgrade of the LBDS, when the SCSS fieldbus is switched to PROFINET.

Many of the gateware IPs designed for this project can now be reused in other projects, as well as some software functions written for the Cortex-M3 processor.

REFERENCES

[1] O. S. Brüning *et al.*, "LHC Design Report", CERN, Geneva, Switzerland, Rep. CERN-2004-003-V-1, Jun. 2004. doi:10.5170/CERN-2004-003-V-1

[2] A. Antoine, E. Carlier, and N. Voumard, "The LHC beam dumping system trigger synchronisation and distribution system", in *Proc. ICALEPCS'05*, Geneva, Switzerland, Oct. 2005, paper PO2.020-2.

[3] L. Allonneau, E. Carlier, and V. Senaj, "Upgrade of the power triggering system of the LHC beam dumping system", in *Proc. PPC'17*, Brighton, UK, Jun. 2017. doi:10.1109/PPC.2017.8291246

[4] N. Magnin, E. Carlier, B. Goddard, V. Mertens, and J. Uythoven, "Internal post operation check system for kicker magnet current waveforms surveillance", in *Proc. ICALEPCS'13*, San Francisco, CA, USA, Oct. 2013, pp. 131–134.

[5] C.B. Durmus, E. Carlier, N. Magnin, and T.D. Mottram, "Spark activity monitoring for LHC beam dump system", presented at ICALEPCS'23, Cape Town, South Africa, Oct. 2023, paper TUPDP099, this conference.

[6] V. Senaj, D.C. Pastor, and T. Kramer, "High performance triggering transformer for stack of series connected thyristors", in *Proc. PPPS'19*, Orlando, FL, USA, Jun. 2019. doi:10.1109/PPPS34859.2019.9009655

[7] N. Magnin, W. Bartmann, C. Bracco, E. Carlier, G. Gräwer, T.D. Mottram, E. Renner, J.P. Rodziewicz, V. Senaj, and C. Wiesner, "Consolidation of re-triggering system of LHC beam dumping system at CERN", in *Proc. ICALEPCS'19*, New York, NY, USA, Oct. 2019, pp. 412–416. doi:10.18429/JACoW-ICALEPCS2019-MOPHA088

[8] P. Van Trappen, E. Carlier, M. Gauthier, N. Magnin, E.J. Oltedal, and J. Schipper, "SoC technology for embedded control and interlocking within fast pulsed systems at CERN", in *Proc. ICALEPCS'19*, New York, NY, USA, Oct. 2019, pp. 592–596. doi:10.18429/JACoW-ICALEPCS2019-MOPHA153

[9] N. Voumard, C. Boucly, M.P. Pimentel, L. Strobino, and P. Van Trappen, "Use of multi-network fieldbus for integration of low-level intelligent controller within control architecture of fast pulsed system at CERN", in *Proc. ICALEPCS'19*, New York, NY, USA, Oct. 2019, pp. 589–591. doi:10.18429/JACoW-ICALEPCS2019-MOPHA152

[10] P. Burr and S. George, "Bringing the benefits of Cortex-M processors to FPGA", presented at Xilinx Developer Forum, Frankfurt, Germany, Dec. 2018.