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FRIB BEAM RAMP PROCESS CHECKER AT CHOPPER MONITOR*

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Abstract

Chopper in the low energy beam line is a key element to control beam power in FRIB. As appropriate functioning of chopper is critical for machine protection for FRIB, an FPGA-based chopper monitoring system was developed to monitor the beam gated pulse at logic level, deflection high voltage level, and induced charge/discharge current levels, and shut off beam promptly at detection of a deviation outside tolerance. Once FRIB beam power reaches a certain level, a cold start beam ramp mode in which the pulse repetition frequency and pulse width are linearly ramped up becomes required to mitigate heat shock to the target at beam restart. Chopper also needs to generate a notch in every machine cycle of 10 ms that is used for beam diagnostics. To overcome the challenges of monitoring such a ramping process and meeting the response time requirement of shutting off beam, two types of process checkers, namely, monitoring at the pulse level and monitoring at the machine cycle level, have been implemented. A pulse look ahead algorithm to calculate the expected range of frequency dips and rises was developed, and a simplified mathematical model suitable for multiple ramp stages was built to calculate expected time parameters of accumulated pulse on time within a given machine cycle. Both will be discussed in detail in this paper, followed by simulation results with FPGA test bench and actual instrument test results with the beam ramp process.

INTRODUCTION

Facility for Rare Isotope Beams (FRIB) has been operating with 5 kW beam power level and in the beam power rump up toward the design beam power of 400 kW [1]. The heavy ion beams accelerated with the driver linac are delivered to a rotating carbon target to generate secondary beams that are used for various experiments. As we increase the beam power, it is becoming more important to control transient heat load to the target to mitigate the risk of damage due to heat shock especially at restart after a beam trip. A chopper in the low energy beam line is a key element to control the beam power. The chopper deflects the beam transversely with high voltage electric field that is generated following the gate signal provided from Global Timing System (GTS), and the deflected beam is stopped at the chopper to generate the beam pulses downstream. The chopper is often used to control the beam power by controlling beam duty factor. Additionally, the chopper generates a notch in every machine cycle of 10 ms for beam diagnostics. Without the diagnostics notch, some beam diagnostics do not function properly including the ones used for machine protection. As appropriate functioning of chopper is critical for machine protection, an FPGA-based chopper monitoring system was developed to monitor the beam gated pulse at logic level, deflection high voltage level, and induced charge/discharge current levels, and shut off beam promptly at detection of a deviation outside tolerance. Once FRIB beam power reaches a certain level, a cold start beam ramp mode which linearly ramps up the pulse repetition frequency (PRF) and pulse width (PW) becomes necessary for beam operation.

The cold start mode starts with the pulse of PW from 0.6 μs to 2 μs and the PRF of 2 kHz. Keeping the PW unchanged, in step one it ramps up PRF from 2 kHz to 25 kHz in 30 s with a fixed rate of 0.77 KHz/s. Keeping PRF unchanged, in step 2 it ramps up PW from its start value to 5 μs in 30 s with a rate of 0.15 μs/s; in step 3 it ramps from 5 μs to 20 μs in 40 s with a rate of 0.38 μs/s; in step 4 ramps from 20 μs to 39.4 μs in 393.6 s with a rate of 0.0493 μs /s. At last, the 25 KHz and 39.4 μs pulse will change to 100 Hz and 9.95 ms which is called full power pulse after a transition period.

The pulses are ramped up within a repeated machine cycle (MC) time structure which starts with a diagnostic notch of 50 μs where no beam is allowed followed by a 9.95 ms period of time where beam is allowed and ramping occurs. As the PRF increases linearly from pulse to pulse, the last pulse of a machine cycle may not fit exactly into the MC. When this is the case, the planned cycle time might be larger or less than the time left of the MC. We will call this fact as “PRF dips or rises” here. In order to keep the duty cycle constant, the PW shall rise or dip along with the PRF as it deviates from its planned value.

Beam power is adjusted using the chopper by changing the beam gated pulse [2]. The chopper monitoring system was developed to check the beam gated pulse from Global Timing System (GTS) at logic level, deflection high voltage level from High Voltage (HV) switch and induced charge and discharge current level from chopper plates [2]. The PW must not be less than 0.6 μs because of the chopper monitor detection speed limit. It is a challenge to design a FPGA logic to be able to monitor such a ramping process and cover various cases of pulse patterns and response the fault in a timely manner.

Two types of ramp-up process checkers, a micro checker monitoring at the pulse level and a macro checker monitoring at the machine cycle level, are implemented in the design. The micro checker can detect a fault at pulse level but is not able to monitor the linear scale over an accumulated time period. The macro checker can detect a fault of linear scale over an accumulated time period but response time is slow since it has to wait for either the counts to reach beyond the expected number or for the end of the examined time period to decide if total counts is less than expected.

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A pulse look ahead algorithm to calculate the expected range of frequency dips and rises of last two pulses close to the end of MC was developed and a simplified math model suitable for multiple ramp stages was built to calculate expected time parameters of accumulated beam on time (BT) within a given machine cycle. Both will be discussed in detail in this paper, followed with results tested with the beam ramp process.

DESIGN

Displayed in Fig. 1, the beam ramp process checker consists of 7 function blocks of pulse counter, micro checker, macro checker, control, Double Data Rate memory (DDR3), microBlaze and physical interface of User Datagram Protocol (UDP) and universal asynchronous receiver / transmitter (UART). The pulse counter block takes the signal from GTS event receiver, HV switch and chopper plate and counts the PW, cycle time of PRF and total beam on time of MC using an 80.5 MHz clock and generates the count done signals of PW, cycle and MC. These counts and done signals are distributed to the micro and macro checkers, where they calculate the range of expected values ahead of time and check if the presented counts exceed the maximum (max) value before the done signal is asserted and if they are less than the minimum (min) value after the done signal is asserted. Fault signals of PW, cycle and beam on time of MC will be triggered if their counts fall out of range. The control block has a timer to assert valid signals of ramp steps, these valid signals enable the micro and macro checker to move to the corresponding ramp stage of initialization and calculation. It packs the data of calculated range, counts and checking results of PW, cycle and beam on time of MC and loads to two DDR3 where each has 256MB memory. It also communicates with the microBlaze to configure the checker with user data and display the related status. The microBlaze system handles the UDP and UART communication protocol. The UDP physical interface is based on Ethernet Serial Gigabit Media Independent Interface (SGMII) core which provides communication channel for Experimental Physics and Industrial Control System (EPICS). UART physical interface is the USB port, which can readout the DDR3 content for debug purposes.

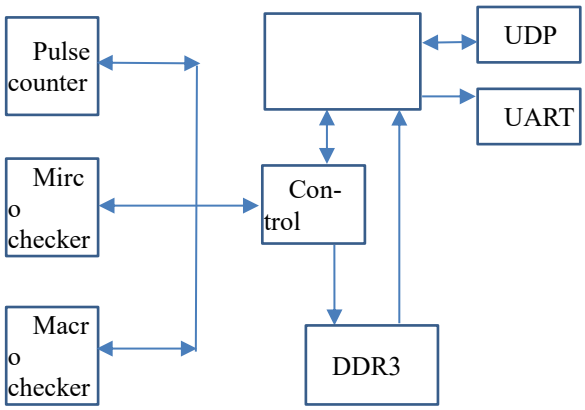

Figure 1: Process checker system block diagram.

Micro checker consists of a micro Digital Signal Processing (DSP) and a look ahead logic block. The micro DSP calculates the max and min target value. It consists of one fixed point to floating point number converter block and two value calculator blocks (one for max, one for min). The converter takes the fixed point number inputs of cycle time, rate and initial value of each ramp step and converts them to floating point numbers for the max and min value calculator blocks. The two calculators calculate the max and min value in parallel with the following equation:

$$FW(n)= FW(n-1)+Rate*Time(n-1)/80500000 \quad (1)$$

$$Cycle(n)= 80500000/FW(n) \quad (2)$$

$$PW(n)\_max1=PW(n-1)*Cycle(n)\_max/Cycle(n)\_min \quad (3)$$

$$PW(n)\_max2=PW(n-1)*Cycle(n)\_ext/Cycle(n)\_min \quad (4)$$

$$PW(n)\_min= PW(n-1)*Cycle(n)\_min/Cycle(n)\_max \quad (5)$$

Where FW(n) is the value of PRF or PW of next pulse; FW(n-1) is the current value; cycle(n) is the cycle value of next pulse; Cycle(n)_max is the max cycle value of next pulse; Cycle(n)_min is the min cycle value of next pulse; Cycle(n)_ext is the extended cycle value of next pulse; time(n-1) is the accumulated time from starts when cycle valid signal is asserted. PW(n)_max1 and PW(n)_max2 are the max PW of next pulse in different cases; PW(n)_min is the min PW of next pulse.

At ramp step1, the micro DSP block is loaded with the initial value of FW(n-1), the accumulated time of Time(n-1) and the rate of 0.77 KHz/s to calculate the max and min PRF with Eq. (1) of the next pulse then derives the corresponding cycle time with Eq. (2) and the max and min PW with Eqs. (4) and (5) to maintain the constant duty cycle rate. The look ahead block calculates the accumulated time by adding the derived max cycle time to the current value of Time and enable DSP block to calculate the 2nd pulse cycle time and PW. The block will decide to maintain, extend or shrink the derived cycle time by comparing it with the time left in the MC. As such, if the time left from the MC is long enough to place the full cycle of 2nd pulse within the bounds of the MC, it will maintain the derived cycle value of the next pulse. If it is not long enough after deduced by the diagnostic notch but enough for the first pulse cycle and PW, then extend the 1st pulse cycle to reach the end of MC. The 1st pulse can be shrunk in case the time left is not long enough to place the full cycle of 1st pulse. The corresponding PW can be decided from Eq. (4) in case cycle is extended, cut back to initial value in case cycle is shrunk.

At the start of ramp steps other than one, FW(n-1) will be loaded with initial value of PW. Time(n-1) is re-counted from the beginning of each step. Rate will be reloaded with expected rate of the step. The expected max and min PW of the next pulse is calculated with Eq. (1). The expected cycle time is always fixed except for the last two pulses of the MC. Like step 1, look ahead logic decides if the last two pulses of the MC need to be extended, shrunk or remain unchanged. All the calculation is completed with a pipelined structure of floating point number operators of

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one multiplier, one divider, one adder and one floating to fixed point number converter. The final value of tolerance is derived by adjusting the calculated value from DSP with the pulse cycle ramp step size, the expected max and min value of transition period and the full power pulse.

The macro checker calculates the tolerance range for the BT of MC and checks if measured BT is within the tolerance range. The expected value of BT comes from Eq. (6).

$$G(T) = \int_0^T F(t)W(t)dt \quad (6)$$

Where G(T) is the gross BT over interval T, F(t) is the PRF at time t, W(t) is the PW at time t. At ramp step 1, F(t) =F(0) + R_f*t, F(0) is the start Frequency, W(t) is the PW of constant W. At other steps, F(t) is constant PRF of F, W(t) = W(0) + R_w*t. W(0) is the start PW. Therefore the G(T) of step 1 can be calculated from Eq. (7), G(T) of other steps can be derived from Eq. (8). The max and min range is calculated from G(T) by adding or subtracting E*T, where E is tolerance per time.

$$G(T) = F(0) * W * T + R_f * T^2 * \frac{1}{2} * W \quad (7)$$

$$G(T) = F * W(0) * T + R_w * T^2 * \frac{1}{2} * F \quad (8)$$

The macro checker DSP is built on one of each floating point number operator of adder, subtractor, multiplier, divider and floating to fixed point number converter, and two of fixed to floating point number converters. The algorithm displayed in Fig. 2 is followed to pipeline these operators and achieve the best balance of FPGA resource utilization and calculation speed.

- S1, initialization, set F(t) and W(t) to initial value.
- S2, calculate increment per second = (F(t) + (R*T/80500000)/2)*W(t). For ramp step 1, load R with frequency ramp rate. For other ramp steps, load R with width ramp rate. Calculate R*T first, then divided by 80500000 and 2 to get the quotient, where T is counts of 80.5MHz clock of one MC. If it is ramp step1, add the quotient to F(t) and multiply with W(t), set F(0) to the value of F(t). If it is in other ramping steps, add the quotient to W(t) and multiply with F(t). Set W(0) = W(t). Where F(0) and W(0) are the value of PRF and PW respectively, at the time when the next MC starts.
- S3, add E to the S2 multiplier result.
- S4, subtract E from S2 result.
- S5, calculate the max target value from S3 adder output by multiplying it by T /80500000.
- S6, calculate the min target value from S3 subtractor output by multiplying it by T /80500000.
- S7, if it is ramp step 1, calculate F(t) =F(0) + R_f*t, if it is any other ramp step, calculate W(t) = W(0) + R_w*t.
- S8, check if the MC counts are within the max and min range and trigger a fault if they are not. Return to S2 and repeat if MC valid signal has arrived.

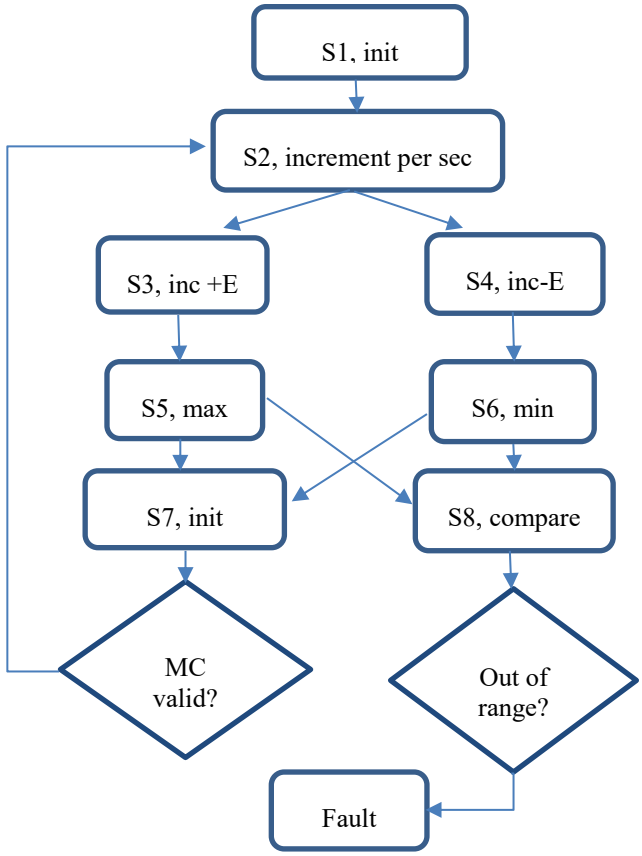

Figure 2: Macro checker DSP flow chart of data processing.

TEST AND RESULTS

The DSPs of micro and macro checker were tested in functional and post route simulations. The DSP is built with pipeline structure and pipeline clock is 80.5 Mhz. Latency of each floating point number operator was selected to achieve high speed and meet the timing requirement of pipeline clock rate. The timing is checked in the post route simulation. The calculation accuracy is checked in the function simulation of the whole ramp process by comparing the calculation results of DSP with the math result from the test bench. Since the ramp rates of steps 2 and 4 are very small and a long simulation period is required to see a significant change, the rate is adjusted to a bigger number to produce a significant result change in a shorter simulation period.

A lab test was conducted to test the entire FPGA design. The pulse source is the GTS pulse generator. The FPGA platform is the FRIB General Purpose Digital Board [2]. The software is the EPICS IOC and OPI of the chopper monitor [2]. Both the micro and macro checkers are required to be configured through the EPICS before the GTS pulse starts. This includes parameters of the micro checker of start pulse width, PRF, their error tolerance and cycle ramp step size and parameters of the macro checker of time period of machine cycle and error tolerance of beam on time integral of each ramping step. The results are checked

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with chipscope and by plotting the measured data stored in DDR3.

The speed of the micro and macro checkers is measured from the start of a calculation when a cycle or MC count done signal is received and new data is available, to the end of the calculation, when results are available. It takes about ~1 µs to get the calculation results.

Fault detection functionality is tested for both checkers. Figs. 3 and 4 display examples where the PW and cycle fault from micro checker are triggered before done signal arrives when presented pulse counts is larger than expected max value. Fault signals are also verified to be triggered only after the counts done signal is pulsed in the case that the counts are less than expected min value.

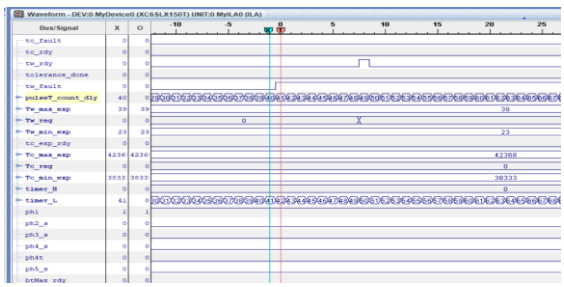

Figure 3: PW fault signal is asserted one clock (80.5 MHz) after presented pulse counter (pulseT_count_dly) is larger than expected maximum value of PW (Tw_max_exp = 39) before PW count done signal is asserted (tw_rdy).

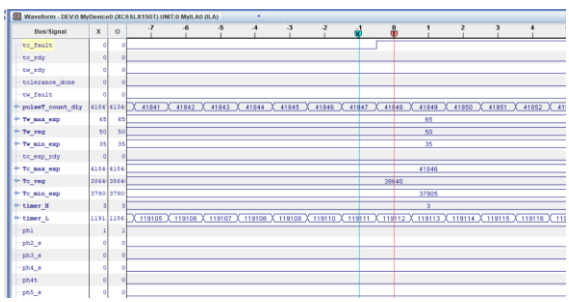

Figure 4: Cycle fault signal is asserted one clock (80.5 MHz) after presented pulse counter (pulseT_count_dly) is larger than expected maximum value of cycle time (Tc_max_exp = 41846) before cycle count done signal is asserted (tc_rdy).

The ramp up data over a 500 s ramp period from GTS, micro and macro checker, which includes the PRF, PW of each pulse and BT of each MC, are plotted from Fig. 5 to 10. The data is read out from DDR3 though the UART port and unpacked in a python program. It can be observed from Fig. 5, at ramp step 1, GTS pulse PRF ramps up through equation of 25/n KHz by reducing n from 14 to 1, total 14 frequencies. In some cases the PRF jumps back from 25KHZ/n to 25KHz/(n+1) at the end of a MC, then change to 25KHZ/(n-1) at the start of the next MC. In most cases 25KHZ/n and 25KHz/(n+1) are interleaved with each other within a MC. At other ramp steps, PW is ramped up linearly according to specification described earlier while the PRF is maintained at 25 KHz most of the time but jumps back to 12.5 KHz on the last pulse of the MC. About ~300ms before the start of full power, 25 KHz pulse with 39.4 µs PW is interleaved 12.5 KHz pulse with 79 µs PW to further increase BT time before finally reaching full power. It can be observed as well that at ramp step 4, the PW of last pulse of MC is cut back by the diagnostic notch.

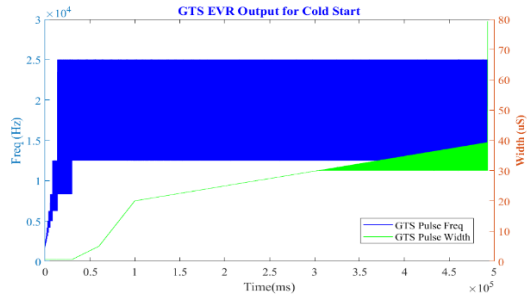

Figure 5: GTS pulse generator output signals, blue signal is the PRF vs. Time. Green signal is the PW vs. time.

The micro checker is configured with pulse cycle ramp step size = 4000 (~50 µs), start pulse width = 49 (0.6 µs), its error tolerance = 10 (0.12 µs), start PRF = 2000 Hz, its error tolerance = 100Hz, the max and min value envelope is plotted in Figs. 6 and 7. From the Fig. 6 plot, it can be observed that the blue curve of input pulse PRF falls into the envelope of max and min value of target PRF. Pulse cycle fault was checked with chipscope during the test and was not detected. From the Fig. 7 plot, it can be observed that the black curve of PW of input pulse falls into the envelope of max and min value of target PW. The PW fault was checked with chipscope during the test and was not detected. These were the expected results.

The look ahead logic function is verified OK. Zoomed in examples at 492.637 s of Figs. 6 and 7 are plotted in Figs. 8 and 9, respectively. It demonstrates that, when time left of the MC is 120 µs, which is not long enough to place 2nd pulse cycle of 40 µs after the time left is subtracted by the diagnostic notch of 50 µs but long enough for the first pulse cycle of 40 µs and PW of 39.4 µs, the 1st look ahead pulse cycle is allowed to be extended to reach the end of MC and becomes 120 µs. Its corresponding PW is extended to 3 times of its planned value. When time left of MC is 80 µs, which is not long enough to place the first look ahead pulse cycle of 40 µs after deduction of diagnostic notch, the cycle time of this pulse will be extended but the PW will be cut back to initial value of 0.6 µs.

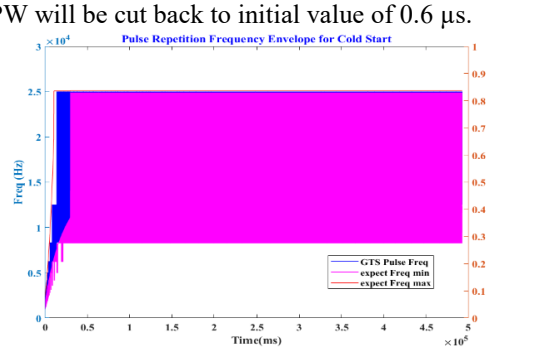

Figure 6: Micro checker calculated range and GTS PRF signal. The blue signal is the GTS PRF, red signal is the expected maximum value of PRF, the magenta signal is the expected minimum value of PRF.

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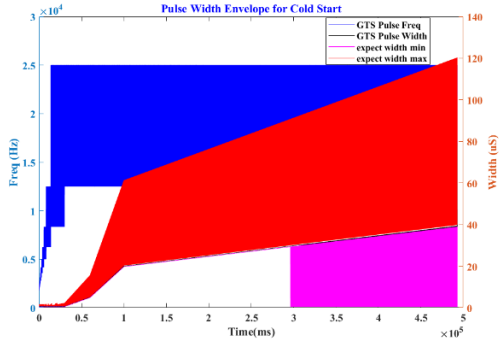

Figure 7: Micro checker calculated range and GTS PM signal. The blue signal is the GTS pulse PRF, black signal is the GTS PM, red signal is the expected maximum value of PM, magenta signal is the expected minimum value of PM.

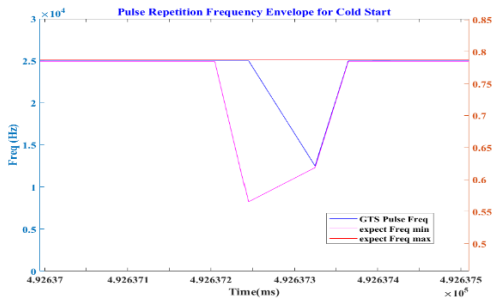

Figure 8: Zoom in at 492.637 s of Fig. 6, the look ahead logics of micro checker usually extend or shrink last two pulses. It allows the pulse to extend the cycle to the end of MC when only 120 and 80 µs left of MC.

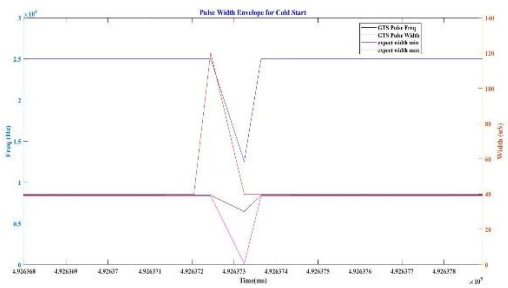

Figure 9: Zoom in at 492.637 s of Fig. 7, the look ahead logics of micro checker usually extend or shrink last two pulses. It allows the pulse to extend the PW to the 3 times when cycle is extend 3 times and shrink to start PM value (0.6 µs) when PW of last pulse is reduced by the diagnostic notch.

The macro checker is configured with time of machine cycle = 805000 (10 ms), error tolerance of BT per MC is 400 counts (~5us) for ramp step 1, 550 counts (6.83us) for ramp step 2, 1900 counts (23.6us) for ramp step 3, 5550 counts (69us) for ramp step 4. The max and min value envelope and actual BT counts is plotted in Fig. 10. It can be observed that the blue curve of BT time counts of MC falls into the envelope formed by red curve of max target value and green curve of min target value, therefore it is not expected that the BT time fault is triggered during the test, this was verified by checking the BT time fault with chipscope.

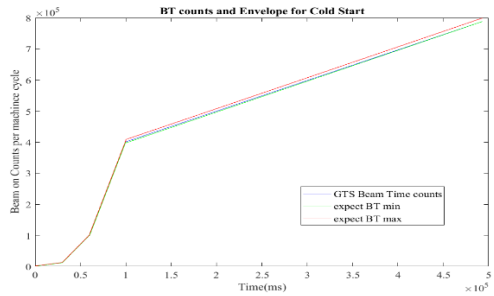

Figure 10: Macro checker calculated range and GTS BT counts per MC. The blue color curve is the BT time counts of MC, red color curve is the expected maximum value of BT time, green color curve is the expected minimum value of BT timer.

CONCLUSIONS

A beam pulse ramp up process checker system was successfully developed at FRIB where the micro checker checks the cycle time and PW of every pulse and macro checker checks BT time counts of every MC. If the pulse parameters fall out of the tolerance envelope, a fault will be triggered and beam will be cut off at the chopper. The process checker is user configurable though the EPICS system and flexible enough to cover various ramp up processes. The ramp up process data is saved in DDR3 memory and can be read out for validation testing and debugging through the UART interface. FPGA function and post route simulation was checked for this design and it meets the function and timing requirements. Lab test with GTS pulse generator was performed and it was verified that all functions work as expected. The future plan is to integrate the beam ramp process checker with other beam mode logics of chopper monitor and the new IOC to be able to read out the process data from DDR3 through UDP interface upon user request and provide more process variables to display the process status and root cause data if a fault is triggered.

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