

TOWARDS DEFINING A SYNCHRONIZATION STANDARD BETWEEN BEAMLINE COMPONENTS AND SYNCHROTRON ACCELERATORS*

X. Serra-Gallifa[†], J. Avila, ALBA Synchrotron Light Source, Barcelona, Spain
R. Hino, ESRF, Grenoble, France
O. H. Seeck, DESY, Hamburg
T. Cobb, DLS, Oxfordshire, United Kingdom
Y. Abiven, S. Zhang, SOLEIL, Gif-sur-Yvette, France

Abstract

Standardization is a magic word in the electronics engineering jargon. Under its umbrella, it is generated the utopia of transparent integration with the rest of the parts with minimal extra effort for the software integration. But the experimental setup in a synchrotron beamline presents multiple challenges: it is highly dynamic and diverse. In the frame of LEAPS-INNOV project (*), the Task 3 of Work Package 5 aims to define a standard for synchronization in the beamline sample environment. Their partners (ALBA, DESY, DLS, ESRF and SOLEIL) have already reached a common vision of synchronization requirements. This paper first details the participants' actual synchronization needs on their facilities. Next, the requirements foreseen for the future are outlined in terms of interfaces, time constraints and compatibility with timing systems. To conclude, we summarize the current state of the project: the hardware interfaces and the hardware platform definition. They both have been decided considering long-term availability, use of standard sub-components, and keeping the compromise between cost, development time, maintenance, reliability, flexibility and performance. This hardware architecture proposal meets the identified requirements. In the future, under the scope of LEAPS-INNOV, a demonstrator will be built, and we will work with the industry for its future commercialization.

THE LEAPS-INNOV PROJECT

LEAPS-INNOV is a Horizon2020 EU-funded project that was granted to the League of European Accelerator-Based Photon Sources (LEAPS) consortium members. It is a pilot project focused on implementing technological developments and improving the research capabilities of the European light sources (synchrotrons and free-electron lasers) by reinforcing their partnership with industry. LEAPS-INNOV project will contribute to solving the technological challenges of the nearly 20 European light sources facilities, especially those related with the complexity increase due to the newest generation of diffraction-limited storage rings synchrotrons and X-ray FELs. This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement no. 101004728.

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[†] xserra@cells.es

The LEAPS-INNOV project is composed the following technology work packages (WP): WP1 - Project Management and Dissemination, WP2 - Development of High Throughput X-ray Spectroscopy Detector System, WP3 - SuperFlat, WP4 - NeXtgrating, WP5 - New positioning and scanning systems for speed and accuracy, WP6 - LIDs, WP7 - Data Reduction and Compression, WP8 - Industrial Innovation through Light Source, WP9 - Innovation by Co-creation to-wards Global Challenges.

TASK 5.3: SYNCHRONIZATION BETWEEN BEAMLINE COMPONENTS

As part of the WP5, the task 3 is a self-contained project with a defined objective, deliverables and milestones.

Objectives

The initial and main goal of task 3 of the WP5 is defining a standard protocol for synchronization in the beamline sample environment. Nonetheless, as a result of shared experiences and needs shared along the group meetings, it was detected that a standard hardware for synchronization was also needed. As a consequence, the working group decided to go beyond and to work also on a standard synchronization equipment in which the standard synchronization protocol would be nested. Both a hardware prototype and the standard protocol will be implemented in a demonstrator experiment in a light source facility at the end of the project.

Deliverables and Milestones

For the tracking of the project the board of the work package defined some deliverables and milestones to achieve.

Deliverable D5.1: Collated Existing Solutions and Future Requirements of Facilities for Beamline Synchronization The first deliverable presented on May 2022 was the sum of the contributions of periodic meetings, where the representatives of participating facilities presented the equipment used for the synchronization on the machine and in the sample environment. Also, participants exposed their needs and requirements for a future synchronization standardization. Most of this work is summarized on the next section of this article.

Milestone M5.4: Definition of the Demonstrator Experiment for Beamline Synchronization The definition of the demonstrator as a final target of the work

package was defined in the June 2023. The demonstrator will be a WaveGate X-ray pulse-picker from the company TXproducts. The pulse-picker is an instrument to pick user-defined X-ray pulses from the bunch train from the X-ray source. To date, the switching time is 100ns. For this a double crystal monochromator is detuned in a synchronized fashion. Synchronization will be done with the bunch clock, the pulse-picker, a sample environment and a detector. A drawing of this demonstrator is shown on Fig. 1.

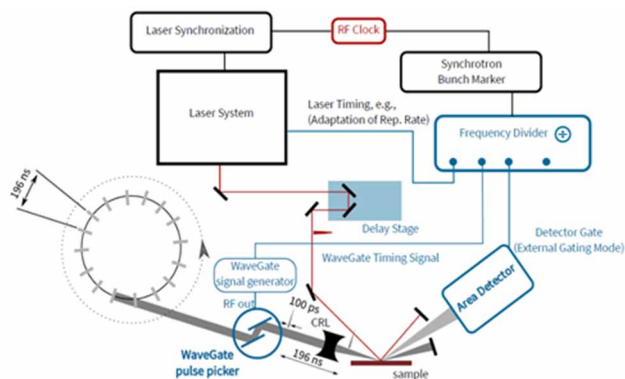


Figure 1: Demonstrator experiment, WaveGate X-Ray pulse-picker.

Deliverable D5.3: Definition of a Standard Protocol for Synchronization between Beamline Components

This deliverable is ongoing and will be presented in the next months. The target is to define a language that could describe the sequences and the close-loops of the beamline components. This language should make easier for the scientists to define the sequences and also to reproduce the experiments on other facilities. The preliminary works done on this deliverable are shown in the “synchronization protocol” section of this article.

Deliverable D5.7: Installation of the Synchronisation Protocol and Demonstrator Experiment at several facilities As already specified in milestone MS5.4, this demonstrator experiment will be working by March 2025, the end of the project. For the achievement of this task, it is wished to enrol private companies that could continue together with the members of LEAPS the work done.

SPECIFICATION OF THE HARDWARE

At the first stages of this project, it came to light that a hardware synchronization device was needed in most of the participants. The reasons varied from each facility, but the obsolescence of already existing solutions and the necessity to improve connectivity and performance can be highlighted. So, the first efforts were focused on the specification of this hardware where many facilities contributed with their specific needs and priorities, arriving to an agreement. Bellow, the reader can find a summary of the different phases of this specification.

Interfaces

The physical connection of the devices will determine its capabilities. So, the definition of interfaces required some

sessions and work to agree on preferred signals and communication interfaces standards and minimal number of ports required. The different facilities’ backgrounds made difficult to find an agreement on the first meetings. However, the work converged in a flexible device with expansion capabilities and standard signals like RS422, used for encoders, or LVTTTL/TTL signals (see Table 1 as a summary of minimum synchronization interfaces agreed).

The need for SFP ports is clear. First, there are experiments that require synchronization with the machine timing system, which is performed by fibre optics. And second, as the White Rabbit protocol can become in the next years a standard for synchronization, it will require also fibre optic connection.

Despite the EtherCAT is not widely used in beamlines nowadays, EtherCAT is slowly becoming a standard on industry automation systems. Many motion control systems use it for multi-axis synchronization and including a synchronization device on the EtherCAT network opens a wide range of possibilities.

Furthermore, other interfaces were required in some specific setups. So, it was agreed to include a FPGA mezzanine Connector (FMC) as expansion port for that specific requirements like ADC, DAC or any other future needs.

Table 1: Required Synchronization Interfaces (Minimal/Optimal)

Requirement	Interface	Quantity
In/Out Encoder	RS422 50MHz	4 / 8
In/Out Trigger	TTL 200MHz	10 / 20
Out Trigger	TTL 30ps del. adj.	2 / 4
FMC Expansion	VITA 57.1 LPC	1 / 2
Timing	SFP	2 / 4
EtherCAT	EtherCAT	1 / 1

One conclusion drawn from the discussions between the facilities: despite some signals are very demanding, most of the signals necessary for synchronization on the beamlines are of low performance. An example is that most of the requirements are encoder readings and TTL signals in the range of microseconds. However, specific cases require counting at high frequencies or generating events synchronously with resolutions of a few picoseconds.

Another aspect is that despite the facilities require the same signals, the connectors and the pinout preferences could strongly differ. For this reason, the idea is to design peripheral boards which adapt common pins of the FPGA to the needed connectors and pinout for each facility. Also, to improve the flexibility, encoders and trigger signals are defined as input/output configurable whenever possible. Clearly, those outputs or inputs with special requirements, like outputs with 30 ps delay adjustment, will not be configurable.

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Machine Timing Systems

In the actual blossom of 4th generation light sources that increase its luminosity and enlarge the light packets, it is foreseen increased for synchronization with the machine timing system. Examples of these needs are the Time-resolved pump-probe experiments, bunch shaping [1] or surface acoustic wave generators [2].

The machine timing systems already implemented in the facilities that participate in the project are: MRF (Micro-Research Finland) used in ALBA, PSI, BESSY, Diamond; Greenfield used in SOLEIL; WR (White Rabbit) used in ESRF; and other systems based on MicroTCA used in XFEL and PETRA III. All of them use fibre optics which could be connected to an SFP port with the appropriate transceiver. Nonetheless, in the case of White Rabbit protocol, additional circuitry is required to recover the machine clock from certain defined data messages, because the recovered clock from fibre optics is stable at a WR frequency.

Hardware Logic Platform

For the logic implementation of this equipment two hardware logics are necessary: First, a processor unit for the high-level features like configuration, data streaming and watchdog. Second, an FPGA for the low-level implementation of the kernel for generating the synchronization sequences.

FPGAs are amazingly flexible and fast, allowing to implement protocols almost in the physical layer. However, this is not the only feature that makes the FPGA more suitable for these applications, they can implement functions in parallel increasing easily the time precision.

In the last years, different products that integrate multi-core Processors, FPGA and all the related ancillary electronics to work as a stand-alone module have appeared in the market. Those COTS products are referred as SOM (System-On-Module) and usually use latest FPGA technologies that integrate in the same silicon dice the Processor and the programmable logic. Examples of this SOM are the KRIA26 from AMD/XILINX and the MARS, MERCURY and ANDROMEDA families from Enclustra, among others. The use of one of these SOM as the central element of the synchronization equipment is the chosen design approach, but the concrete selected model is still under discussion.

Form Factor

The form factor of this device is again conditioned by the equipment currently in use in each facility to ease the substitution of old equipment. While the preferred form factor is 19" 1U with interfaces in the front and the rear panels, some facilities are interested in a 3U half rack form factor to be installed off a rack in case it is needed. These form factors are drawn on the Figs. 2 and 3.

For that reason, the first conceptual design of the equipment is compatible with both preferences by using a

modular approach. Below the reader can see outlines of the design in both cases.

The electronics distribution design proposal is composed by: a power supply unit (PSU), baseboard, a system on module (SOM), a front panel interface board and a rear panel interface board.

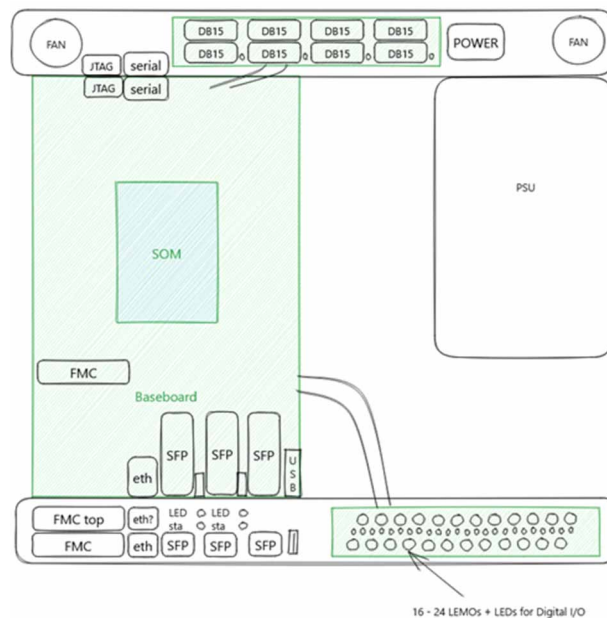


Figure 2: 19" width 1U form factor.

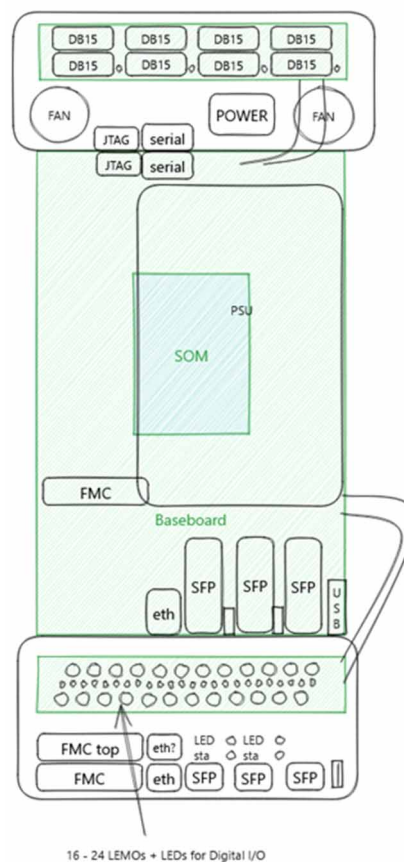


Figure 3: Half 19" rack width 3U form factor.

SYNCHRONISATION PROTOCOL

The synchronization is intrinsically linked to any experiment. However, in the last years the brilliance increase and the improvements in the detectors speed have led to an increase of fast experiments requiring continuous scans or fly-scans. These measurements, done without stopping the actuators during data acquisition, require a synchronization which requires of demanding time-precision. Moreover, nowadays, it is more common to require the flexibility to change the synchronization parameters, even during the experiment. In addition to the time precision and the flexibility, the need to do the same experiment in different facilities is key for the scientists. This involves a challenge for the support groups as the sample environments are different in many aspects between facilities: the synchronisation hardware, the motion controllers, and mainly the SCADA (supervisory and control data acquisition) system. Many efforts are put into simplifying and homogenising the data acquired, but not in the experiment preparation and definition.

One of the targets of this work package is to define a protocol that describes the experiment common to all the facilities. Using a common hardware will ease the definition of a hardware abstraction layer which should allow the implementation of experiments synchronization and the communication between synchronization devices.

Hardware Synchronization Protocol

The hardware device described previously, will need to implement a firmware supporting all the available flexibility. For that reason, it should be implemented non-monolithically, based on functionality blocks that will be implemented depending of the interfaces included on the expansion ports. On different members' facilities, there are solutions already implemented, like the PandABox [3] and the ALBA Em# [4], which face the requirements in different perspectives.

PandABlocks is a firmware that runs on the PandABox and other future Panda products. It consists of statically defined Blocks (like position compare or pulse generator) with inputs, outputs and runtime configurable parameters (like delay or width). The outputs of all Blocks form a wide bus clocked at 125 MHz, and inputs are selected from that bus using multiplexors. This means any Block can be connected to any other Block at runtime, with data taking 8ns to flow between Blocks. The Zynq 7-series which powers the current generation of PandABox limits the width of the bus to 32x 32-bit integers and 128 booleans, but larger FPGAs would allow a wider bus. ALBA Em# firmware is based on Harmony bus, which is a 64 bits bus at 125 MHz (FPGA Clock) were the individual modules place the data with 8-bit identifier and Timestamp. The software configures each of the modules to perform the specified functionality. It is an architecture that not only allows synchronization, but also close-loops feedbacks and ADC data acquisition implementations. Due to the use of a bus, the system is easily scalable, but it is slow on the range of the microsecond response time.

Hardware

Timing Systems & Synchronisation

User Synchronization Description

Many elements require synchronization. Most of them require synchronisation above seconds that can be either done by a human or high-level software. Some of them need a synchronization above milliseconds, which can be done by software. And finally few require more accurate synchronization. This tendency also applies from milliseconds to picoseconds: it is rare to have picosecond requirements in a synchrotron beamline. A graphical representation of this is shown on Fig. 4. On the other side, what is more required is the flexibility and the capability to modify the synchronization parameters. Due to the intrinsic working schema of the synchrotrons, where beamtime is offered in slots to external users, the experiments could require a completely different synchronization scheme.

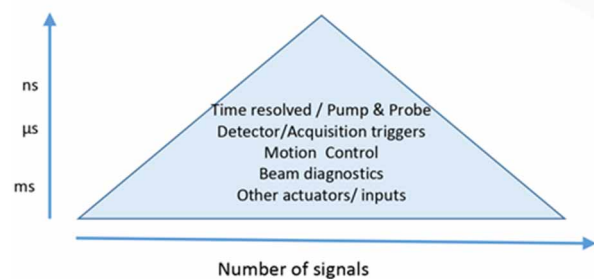


Figure 4: Relation between time precision signals and its quantity.

The protocol must allow to describe the synchronisation needs in every range of time. Moreover, it must be easy to define the experiment for the users, ideally with the use of a graphical tool. On the other hand it must be interpreted by the SCADA systems and by all the agents involved in the synchronization.

CONCLUSION

Synergies between different synchrotron facilities have emerged from the study for a common solution for synchronization in the sample environment. Currently there is a need of an equipment capable to go beyond with the current synchronization capabilities, in terms of number of interfaces and time precision requirements. After fixing the interfaces, the time for designing the HW has arrived. The selection of a SOM, in which all the peripherals will be connected, is the next step. Another need is the creation of a synchronization protocol that would improve for the users the synchronization setting-up and would facilitate the experiment replication in different sample environments. While this protocol definition is still in an early stage, the project will focus, as a necessary first step, now on adopting synchronization protocols internally to the FPGA.

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