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STATUS OF THE MICROTCA BASED BEAM INSTRUMENTATION DAQ SYSTEMS AT GSI AND FAIR

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Abstract

While the first FAIR accelerator buildings are soon to be completed, MicroTCA-based data acquisition systems for FAIR beam instrumentation are ready for use. By using commercial off-the-shelf components as well as open hardware with in-house expertise in FPGA programming, there are now DAQ solutions for almost all major detector systems in MicroTCA in operation at the existing GSI accelerators. Applications span a wide range of detector systems and hardware, often taking advantage of the high channel density and data transmission bandwidth available with MicroTCA. All DAQ systems are synchronised and triggered using a comprehensive White-Rabbit-based timing system. This allows correlation of the data from the distributed acquisition systems on a nanosecond scale.

In this paper, we present some examples of our DAQ implemented in MicroTCA covering the range of beam current, tune, position and profile measurements. While the latter uses GigE cameras in combination with scintillating screens, the other applications are based on ADCs with different sampling frequencies between 125 MSa/s up to 2.5 GSa/s or latching scalers with up to 10 MHz latching frequency.

INTRODUCTION

Already at the beginning of the planning of the FAIR project in 2008, there were efforts in the GSI Beam Instrumentation department to replace the proven but old standard form factor VME. A new hardware basis was required which should provide the following features:

- Higher data bandwidth on backplane
- State-of-the-art bus systems like PCIe (3rd Gen. or higher)
- Modularity (including power supply and fan trays)
- Hot swap or hot plug support
- Availability of relevant components, such as ADC, TDC, counter, I/O or carrier boards for other standard mezzanine technologies, e.g. FMC
- Scalability
- Extensive possibilities for remote maintenance
- High availability

In addition, the new platform should be based on an industry standard and be available as commercial off-the-shelf (COTS) products on the open market, at best with a second source.

During this period, DESY had evaluated the MicroTelecommunications Computing Architecture (µTCA or MicroTCA) form factor for data acquisition at the XFEL and extended the PICMG standard by MTCA.4 for Physics, thus procuring a viable alternative to VME. DESY has significantly advanced the positive development and establishment of the standard through numerous MicroTCA workshops [1], tutorials and the founding of the MicroTCA Technology Lab. The resulting growth of the community led to a stabilization and further development of the standard. With the momentum gained, MicroTCA has become a reliable and powerful option.

Therefore, GSI/FAIR Beam Instrumentation department now uses MicroTCA as its multi-channel data acquisition (DAQ) platform, complemented by Industrial-PC solutions for readout with a small number of channels. It is worth mentioning that our industry partners have also developed, partly at their own financial risk, MicroTCA modules, so-called advanced mezzanine cards (AMC), for specific FAIR measurement tasks. These are now available to everyone on the market.

The FAIR project schedule allowed various beam diagnostic systems at the existing GSI accelerator facility to be upgraded with MicroTCA systems, including integration into the FESA-based control system [2]. After completion of the FAIR facility, stable and mature systems can be quickly installed by simple duplication.

MAIN SYSTEM SETUP

In most applications, a space-saving 2U - 6 slot Schroff (nVent) MTCA.4 chassis (RackPak/M5-1) with standard backplane and 600W or 1000W (AC) power supply is used. In few cases, where a higher number of AMC modules is required Schroff (nVent) 9U - 12 slot crates (RackPak/M12-41) with 1000 W (AC) power supply can be used. Each system requires a MicroTCA carrier hub (MCH, here NAT-MCH-PHYS80), which acts as an interface for remote maintenance and system configuration/control, as well as an internal PCIe and LAN switch. The systems are equipped with a Concurrent Technologies AM-G64 AMC CPU providing Dual PCIe x4 support on AMC ports 4-7 (FatPipe1) and 8-11 (FatPipe2) and a Quad-Core Xeon E3-1505M processor. Both crate types are equipped with a JTAG Switch Module (JSM) slot for FPGA programming via the backplane.

FAIR Timing Receiver Node

The control system design for FAIR is based on a new machine timing system, which was developed by GSI, CERN and other partners on top of the White-Rabbit Protocol [3]. So-called FAIR Timing Receiver Nodes (FTRN) were developed for the targeted standards MicroTCA (AMC=Advanced Mezzanine Card) and PCIe. The development was carried out by Cosylab as an in-kind contribution of Slovenia to FAIR with support of the GSI timing group. The entire product is published under the CERN

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Open Hardware OHL license [4]. The essential features of our FTRN modules for MicroTCA (see Fig. 1) are:

- Five bi-directional LVTTL I/Os used for external trigger input or clock/pulse/gate output
- Eight lines for clock/pulse/gate signals over the backplane (via M-LVDS lines in MTCA.4)
- Internal clock (synchronization across facility in sub-ns precision)
- Event deadlines, timestamps and definition for I/O and software actions at 1 ns LSB
- Execution of programmable actions like real-time signal generation on the I/O or M-LVDS lines or software interrupts for the data acquisition depending on machine events
- Compatibility with Libera Hadron B 1

Figure 1: FAIR Timing Receiver Node (FTRN) in AMC form factor.

CRYRING@ESR BEAM POSITION MONITORING SYSTEM

At GSI, the new low-energy CRYRING@ESR experiment facility, a Swedish in-kind contribution to the FAIR project based on the former CRYRING, hosted until 2013 at Manne Siegbahn Laboratory Stockholm, is used as a testbed for the future beam instrumentation and FAIR control system concepts.

Besides many other measurement systems CRYRING is equipped with 18 beam position monitors (BPM), here 9 horizontal and 9 vertical detectors, for which a new DAQ was developed [5]. The BPMs are designed as diagonally cut cylinders with linear response to beam offsets. The beam position can therefore be calculated by using the difference-over-sum method. Signal processing after digitization includes a running average filter for signal smoothing, a Chebyshev filter for noise reduction as well as a correction for deviations of the plate capacitances.

[1] Libera Hadron B from www.i-tech.si is used at GSI and FAIR for all BPM systems except at CRYRING@ESR. This DAQ system is based on MicroTCA technology with slight deviations to the standard.

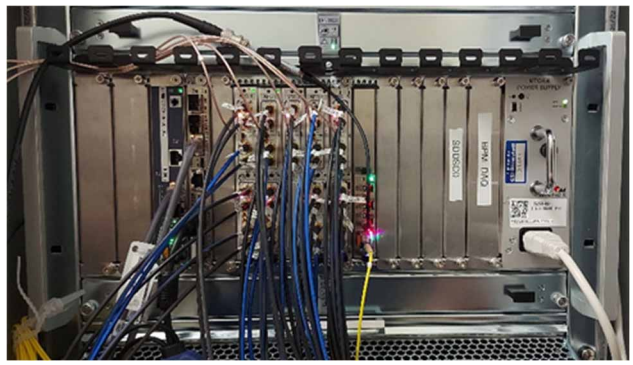

Figure 2: CRYRING@ESR Beam Position Monitoring system using AFC V4 FMC carrier modules with 250MSPS/4Ch/16 Bit ADC FMCs.

Acquisition Hardware

At RF frequencies up to 2.5 MHz it was decided to perform the signal processing and position calculation in an FPGA. Here, the FPGA mezzanine card (FMC) technology was selected for this BPM system in order to gain experience with the VITA standard [6] as the use of FMCs significantly expands the possibilities of DAQ systems.

A reliable, state-of-the-art and high-performance ADC in FMC form factor, was chosen. The hardware consists of five AMC FMC Carriers (AFC-V3.1, ARTIX 7 FPGA) equipped with two 250 MSa/s, 16 bit, 4 channel ADC FMC boards each. Both, carriers and ADCs are published under Open Hardware license (OHL) and were developed in cooperation between the Brazilian Synchrotron Light Source (LNLS) and the Warsaw University of Technology (WUT). The boards are housed together with the AMC FTRN and the CPU in a 12-slot MTCA.4 chassis (see Fig. 2).

DAQ Concept

By settling for an FPGA approach to perform the position evaluation, it was necessary to develop custom gateware. This represented an additional major effort, but it allowed the individual customization of the DAQ to all requirements.

The main working modes provided by the FPGA gateware are three different data streams stored at individual sections of the on-board SDRAM:

- Raw ADC data
- Position data
- Averaged position data

All data streams are triggered by a gate signal generated by the FTRN. The analog signals are digitized at 125 MSa/s. A maximum of 1 GByte of the corrected raw data can be stored per AMC carrier, i.e. 4 BPMs or 8 signals. This corresponds to a maximum acquisition window of 0.537 s. The raw data is usually used to evaluate the signal quality of each BPM and at injection where BPMs are used as beam loss monitors.

A least square algorithm is used to evaluate the position of the beam from the raw data, and makes additional offset correction unnecessary, as this fit reliably reproduces the position regardless of voltage offsets. Per AMC carrier 224 of these turn-by-turn positions can be stored on-board. This

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allows to monitor fast changes in the position over a few minutes.

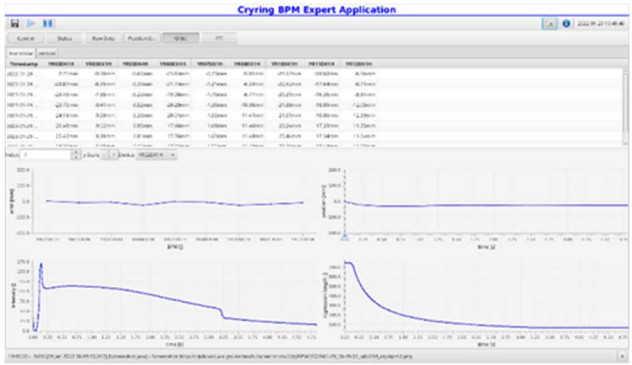

Figure 3: Cryring BPM data, here orbit tab with global orbit (hor.), BPM intensity and position, and fit length (regression).

For monitoring slower position changes in the beam position over longer periods, averaged turn-by-turn positions (orbit data) are stored in the remaining SDRAM.

The DAQ reads out the SDRAM per accelerator cycle and presents the data to the users (see Fig. 3). This is complemented by a client-side FFT for one horizontal and one vertical BPM on the turn-by-turn position data for tune measurement.

Looking at the selection of DAQ hardware made for this BPM system, it can now be judged that the Open Hardware components offer a reliable, cost-effective DAQ solution whose openly accessible schematics and documentation allow full customization to the project's requirements.

FAST CURRENT TRANSFORMER

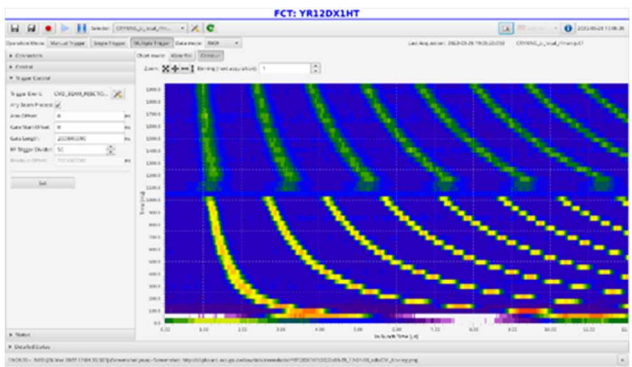

Figure 4: Li+ beam from local injector over 2 seconds from injection to flattop with rebunching from h=8 to h=6 to reduce the maximum RF frequency (middle, Cryring@ESR).

The Fast Current Transformers (FCT) are mainly used at GSI and future FAIR synchrotrons, but also at the high energy beam transfer sections (HEBT) for fast extracted ion beams [7]. Besides beam intensity measurement, they allow for precise determination of the longitudinal bunch structure (see Fig. 4). FCTs are available with analog bandwidth ranging from 300 MHz up to 1 GHz. By means of the SIS8160 / SFMC01 combination from Struck Innovative Systeme (SIS), a dual slot FMC carrier with 2-channel 2.5 GSPS@14-bit FMC ADC, all measurement requirements could be met. At these sample rates the MicroTCA system is well chosen as it provides for highest data bandwidth on the readout with performant data handling in the Xeon CPU. For measurements in the synchrotrons the ADC is operated in the multi-event-mode with precise time stamping of the data packets. Each measurement is triggered by bunch synchronous RF based triggers derived from the SIS18 RF master oscillator. The trigger rate is usually reduced with the aid of a rate divider, which was implemented on a CERN made OHL 5 channel digital I/O FMC module and custom gateware developed in-house. Finally, a SIS8864 multipurpose 64-bit AMC I/O module is used to control the front-end electronics (attenuator and FEMTO DUPVA amplifier) with gains in the range [-60 dB, 60 dB]. This enables the measurement of current and pulse shape as a function of time.

RESONANT TRANSFORMER

Resonant transformers (RT) are used to measure the intensities of fast extracted ion beams (max. 2 µs bunch length) in the transfer sections. RTs developed and manufactured by GSI are based on the excitation of a damped oscillation of the passing ion beam inside the RT electronic circuit [8].

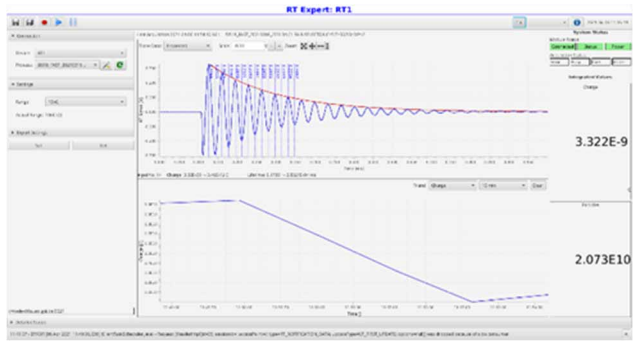

Figure 5: Typical resonant intensity signal using a resonant transformer with fast extracted ion beam.

Older readout of the RTs is based on a peak detector for the first peak of the oscillation and digitization of its amplitude. To reduce noise, the FAIR DAQ will digitize and analyze the damped oscillation (see Fig. 5). For this a combination of AFC V4.1 and a 100 MSa/s 14-bit 4 channel FMC ADC by CERN, both licensed under OHL, was chosen. After acquiring the signal, an FFT is used to suppress the DC offset and high frequency noise. Subsequently, the amplitude of each oscillation is evaluated and fitted against a decaying exponential function. The value of this function at the first maximum is a measure of the charge passing through the RT.

The fine granularity of the timing zones in the FAIR machine timing system is often disadvantageous in the light of the high ADC channel density with a single trigger. Here, the possibility to distribute trigger signals from the FTRN via the eight backplane M-LVDS lines offered by the MTCA.4 standard could be fully used. A custom gateware for the FPGA has been developed which allowed each

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ADC channel to be triggered independently. Furthermore, the trigger for each channel can be individually assigned to any one of the eight M-LVDS lines or the front panel input of the FMC.

This provides maximum flexibility in triggering and the system can also be used as a general-purpose ADC for other DAQ applications.

PARTICLE COUNTER APPLICATION

As described in [9], particle counters at GSI and FAIR are read out for common accelerator operation with the LASSIE system. This multi-channel application is based on MicroTCA counter modules (SIS8800). The dedicated LASSIE graphical user interface displays the measured intensities of the detectors as a function of time. Latching frequencies (time-slice generation) of 1 kHz are usually used for this purpose (see Fig. 6).

However, higher latching frequencies are required to investigate the spill micro-structure at slow beam extraction from the heavy-ion synchrotron among other potential applications. For this purpose, a LASSIE Expert System is currently in development, which is strictly optimized for performance, efficiency and throughput.

As with the Lassie system, Struck MicroTCA SIS8800 multiscaler modules are used. Data acquisition runs continuously and untriggered in the scaler-specific so-called Multichannel Scaler Mode (MCS) and allows for user-space DMA reads from the 2 GB DDR3 on-board memory.

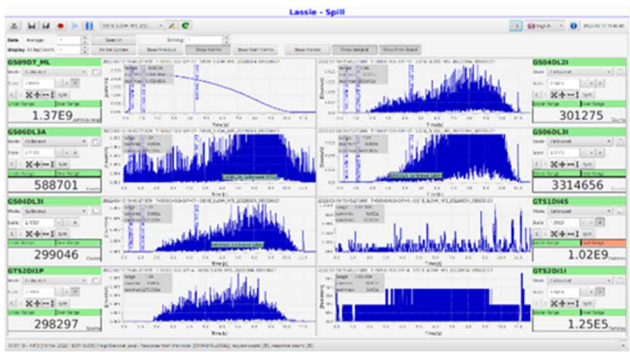

Figure 6: GUI view of the LASSIE intensity measurement with particle detectors.

All acquired data is synchronized with the FTRN clock. In parallel, all timing messages broadcasted at the facility are recorded directly from the UDP stream, bypassing the FTRN. The event messages are placed in the header of the appropriate data frames. This allows full correlation of timing events with the latched data, and makes it possible to evaluate regions of interest across all accelerator sequences and processes at runtime and offline – per channel. It is worth to mention, this provides the advantage of being able to reevaluate regions of interest and correlation between channels of recorded data, as all information is present. This includes taking into account timing events that have not been used at runtime but might prove helpful later on.

Latch-perfect precision between different data channels and absolute timestamping is guaranteed – also across different scaler modules and even different LASSIE expert setups distributed over the campus.

High efficiency and performance is achieved by a pipelined concept similar to what is outlined in [10]. Each pipeline stage is a separate thread. Data is passed from stage to stage by references to segmented memory using fast thread-safe FIFO queues, reducing copy overhead to a minimum. At the same time, the blocking readout from the queues provide implicit synchronization of the pipeline stages. The DAQ instantiates one pipeline per scaler module.

Current working target is a maximum latching rate of 10 MHz and 128 channels simultaneously. On user change of the latching clock, depending on the actual rate, pipelines are reconfigured by specializing to an appropriate data word length (8, 16 or 32 bits) and resynchronized. This reduces unnecessary data overhead significantly without introducing limitations to the DAQ. Extensive quality analysis tools are foreseen, including but not limited to

- Spill duty-factor evaluation
- Total FFT of user-defined regions of interest, such as the spill of slow extracted beams
- Spectrogram with user-defined time slices

Evaluation tools like the duty factor provide a quality measure regarding the spill micro-structure, whereas the FFT is used to determine the optimal operating points for e.g. knock-out extraction from the heavy-ion synchrotron.

SCINTILLATING SCREENS

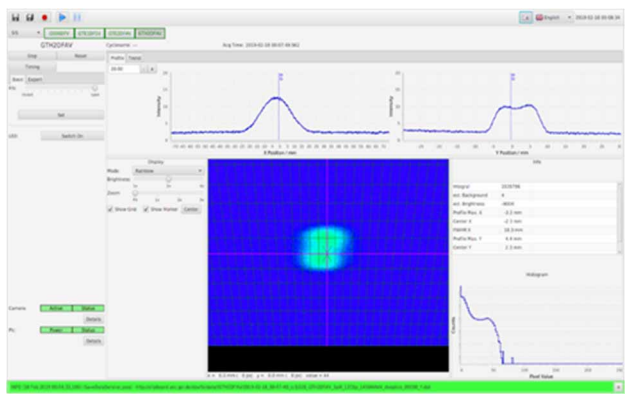

Figure 7: Screenshot of a beam spot on a scintillating screen with data evaluation like projections, FWHM, center of mass etc.

Viewing screens [11] are used to measure transversal distribution of the particle beam (see Fig. 7). With this measuring method, a screen is moved into the beam path at an angle of 45° and observed by a GigE camera. In the DAQ relevant parameters, such as horizontal and vertical projections, center of mass, etc. of the obtained profile are calculated including corrections for perspective using a projection matrix. More complex image data evaluation like higher moments of the beam distribution for automatic beam steering is currently being worked on.

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As this is a beam-intercepting measurement method, it is not necessary to read out several cameras at the same time in a given beam path. The MicroTCA form factor together with an 8 port GigE switch (Vadatech AMC217, see Fig. 8) provides a very compact and performant solution for up to 8 GigE cameras per crate.

Figure 8: MTCA.4 DAQ system for GigE camera readout.

However, a dedicated configuration of the system is required. It is necessary to enable the internal port based VLAN configuration of the NAT-MCH to create a private subnet to shield the GbE cameras from the parent accelerator network and its RADIUS server based network MAC authentication service.

OUTLOOK

Gradually, various beam diagnostic systems at the existing GSI facility are and will be replaced by state-of-the-art MicroTCA DAQ concepts. The focus here is currently on multi-channel applications at the UNILAC (UNIversal Linear ACcelerator), where White-Rabbit timing is still in the trial phase and trigger concepts still have to be evaluated. At present, the UNIMON system is being put into operation for the operating team, which displays the status of approx. 40 relevant RF signals. These are mainly UNILAC structures like IH, RFQ, and Alvarez tanks, but also chopper and buncher signals among others. These signals are displayed online at the UNILAC frequency of 50 Hz. IOXOS 20 Ch/5 MSPS ADC-FMC boards on AFC carriers are used here again with in-house made custom FPGA firmware.

For transmission and beam-loss monitoring, the UNILAC intensity measurement system MAPS is currently replaced by a successor. Four to five TEWS TAMC532 32-channel ADCs at 50 MSPS/16 bit, reduced to 10 MSPS, simultaneously digitise all 64 UNILAC AC transformers including their special frame pulses provided by the chopper unit. The challenge here is that triggers, depending on the respective accelerator section, are distributed over a high number of timing domains. This makes it difficult to group the individual ADC channels appropriately. First tests of both systems are scheduled for the beam time in November this year.

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