OVERVIEW AND OUTLOOK OF FPGA BASED HARDWARE SOLUTIONS FOR DATA SYNCHRONIZATION, ACQUISITION AND PROCESSING AT THE EuXFEL

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Abstract

The European X-Ray Free Electron Laser facility (EuXFEL) provides ultra short coherent X-Ray flashes, spaced by 220 nanoseconds and with a duration of less than 100 femtoseconds, in bursts of up to 2700 pulses every 100 ms to several instruments. The facility has been using standardized Field-Programmable Gate Array (FPGA) based hardware platforms since the beginning of user operation in 2017. These are used for timing distribution, data processing from large 2D detectors, high speed digitizers for acquisition and processing of pulse signals, monitoring beam characteristics, and low latency communication protocol for pulse data vetoing and Machine Protection System (MPS).

Our experience grows in tandem with user requests for more specific and challenging case studies, leading to tailor made hardware algorithms and setups. In some cases, these can be fulfilled with the integration of new hardware, where collaboration with companies for new and/or updated platforms is a key factor, or taking advantage of unused features in current setups.

In this overview, we present the FPGA hardware based solutions used to fulfill EuXFEL's requirements. We also present our efforts in integrating new solutions and possible development directions, including Machine Learning (ML) research, with the aim of bringing more accurate results and configurable setups to user experiments and facilitate communications with other platforms used in the facility, namely Programmable Logic Controllers (PLC).

INTRODUCTION

Located in Hamburg, Germany, the European X-Ray Free-Electron Laser facility (EuXFEL) provides ultra short coherent X-Ray flashes for scientific applications. These bunches have an energy between 260 eV and 24 keV and can be generated at a repetition rate up to 4.5 MHz for 600 µs [1]. A new batch of pulses, referred to as a train, is generated every 100 ms and distributed among the seven instruments currently operating at EuXFEL. Additionally, synchronized optical laser pulses are available to all instruments for time-resolved pump-probe studies and laser-controlled manipulation of electronic relaxation and excitation processes. These instruments use the properties of the generated pulses for a wide range of scientific research topics.

Bandwidths of 10 GBytes of data per second are generated from the unique 2D pixel detectors available in the facility, while detector types, like systems based on fast digitizing and

analog-to-digital converters, can reach up to 70 MBytes. The latter detectors are used not just for scientific experiments, but also for diagnostics purposes. Besides the data volume, synchronization with the main accelerator is a key aspect in the setup of the experiments.

Considering the variety of experiments that take place at the EuXFEL, together with the ever-changing user requirements and high-speed data throughput, the facility requires a hardware framework which can cope with the expected data bandwidth while offering flexibility, scalability and processing features to reduce the amount of data to be store.

Field Programmable Gate Array (FPGA) technology provides the simple hardware solutions together with the ability to implement functions during the firmware programming phase. The technology is relevant in data processing, allowing for reduction and filtering to be done at the hardware level together with implementation of low-latency feedback systems. Algorithms can be continuously upgraded without having to change the hardware, and the code reused and easily integrate into different projects.

HARDWARE PLATFORMS

The main hardware platform is based on MicroTCA.4, a modular, open standard, created and maintained by the PCI Industrial Computer Manufacturers Group (PICMG) [2]. It provides its compatible boards, refer to as Advanced Mezzanine Cards (AMCs), high-speed interconnects via PCIe, Ethernet and point-to-point, with redundant cooling and power supply as well as full remote monitoring, control and automatic failure detection and reaction. These are particularly important for the EuXFEL, due to the many decentralized locations where sensitive measurement signals are detected and timing signals are required. The MicroTCA.4 standard extends the AMC card definition with a Rear Transition Module (RTM), a second board physically connected to the AMC to extend the amount of I/O. Other relevant and standard features of the platform include the possibility to distribute signals and clocks between the AMCs via the backplane, i.e. without the need for external equipment, and a MicroTCA Carrier Hub (MCH) which is the central managing device of a MicroTCA crate.

Based on this platform, we use FPGA equiped AMCs which provide digitization, synchronization, online processing and realtime data rejection (vetoing) capabilities. Commercial and custom design RTMs extend the functionality of these integrated AMCs to address the instruments' setup requirements. CPU AMCs allow for remote configuration, monitor and collection of the data acquire by the other AMCs

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present in a MicroTCA crate. Processing of data can also occur in these CPUs before transmitting it to external storage.

In the following sections we offer a brief description of AMC boards integrated at the EuXFEL (as shown in Figure 1), custom FPGA developments, and tools used for deployment and monitoring of equipment.
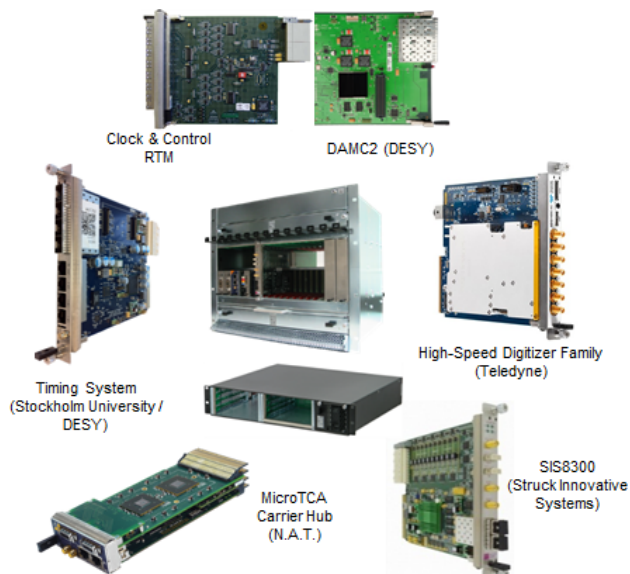

Figure 1: MicroTCA crates and some of the AMCs integrated at EuXFEL.

OS Deployment and Configuration

MicroTCA crates are installed in tunnels' photon beamlines and in the scientific instruments. To ensure conformity across all CPUs AMC, and to simplify the installation process, Foreman [3] and Puppet [4] tools are used for OS and Software deployment respectively. The former installs the OS, based on an image maintained by EuXFEL, via ethernet by using the PCIe Boot feature available in the CPU's bios. The tool takes into account the manufacturer and architecture and its usage e.g. production, development or testing. Puppet takes care of users and groups rights access definition, packages, drivers as well as system tools, guaranteeing that all systems have the same environment. Custom Puppet code also takes care of configuration of servers and tools which are specific for EuXFEL. When special software setups are required, Puppet allows to specify different configuration values according to host, host-groups or locations.

Monitoring and Alarm Tools

For monitoring and alarm services, we are currently using Nagios software [5]. The tool periodically checks relevant information of the CPU host, such as temperature, hard disk usage and load, availability, and generates and email and/or an SMS when the monitored parameters are not within limits. Rrsyslog [6] is also used to monitor the activity taking place in the host.

Distributed Object-Oriented Control System (DOOCS) [7] servers installed at DESY, the institute responsible for the accelerator, collected via the MCHs data concerning the temperature, availability, and connectivity of all AMCs present in a crate, and are displayed in JDDD panels [8]. Whenever an event is logged in the MCH, an email is sent to a mailing list informing of the occurrence.

Timing and Synchronization

The European XFEL Timing System is implemented in a MicroTCA AMC developed within a collaboration between DESY and Stockholm University [9,10]. This board, equipped with an FPGA, provides accurate and stable triggers to synchronize acquisition, provide reference frequencies (clocks) to align sampling rates and other sequencing clocks in frequency and phase as well as to distribute train information and other parameters in a deterministic way.

The main signal is encoded and distributed over fiber cables to all timing systems in the experiment stations and photon beamlines, covering a distance of over three kilometers. Propagation delay of the fiber cables, temperatures of critical electrical components and phases of different clocks are constantly monitored and compensated. Decoded triggers and clocks are delivered to local AMCs via the MicroTCA backplane or to external equipment. We developed two standard adapter boxes, one to convert LVDS (Low-Voltage Differential Signaling) trigger and clock outputs of the AMC into TTL (Transistor-Transistor Logic), and one in the opposite direction for special interlock inputs of the AMC.

Train information distributed include an unique number associated with that train (refer to as Train ID), beam mode per section and a table which contains the information of all bunches (availability, charge, destination...). This information is available in all timing system modules before any train is generated and is further distributed to all AMCs in a MicroTCA crate and external equipment, like our PLC system. We have also developed an USB solution to retrieve this information for user equipment that is not integrated in the data acquisition flow at EuXFEL.

Digitizers AMC

Besides timing, the most common applications where the MicroTCA platform is utilized, are AMCs to digitize analogue signals from detectors (e.g. (avalanche) photo diodes, diamond plates, multi-channel plates). Depending on the relevant properties of the transient signals (e.g. energy of a pulse, peak time of a pulse, shape of the signal) different signal shaping, sampling rates, resolution and processing requirements have to be maintained or provided.

For transient signals with a bandwidth below 100 MHz or interest in the energy of pulses, we have integrated the SIS8300 from Struck Innovative Systems [11]. It provides 10 channels of up to 125 MSPS with 16 bit nominal resolution. Two different RTM modules are used for this AMC: the commercially available SIS8900 also from Struck and an in-house developed that is able to stretch the analogue signal before it is digitized, allowing the processing of pulses with

a width shorter than the sampling period. The AMC also includes an FPGA as central element, running a custom firmware developed by EuXFEL.

For peak time detection of fast pulses and spectral information of moderate time-of-flight signals, the AMC ADQ412-4G-MTCA from Teledyne was selected [12]. This 12 bit resolution AMC provides 4 channels with up to 2 GSPS or 2 channels with up to 4 GSPS (software configurable). The board is provided with an FPGA firmware, however a user space is available for signal processing and data handling.

To address the need of higher resolution digitizers, we are investigating options currently available in the market, including the new generation of Teledyne's ADQ7 AMC modules, which can provide up to 10GSPS with 14 bit resolution. While faster sampling solutions are available (e.g. 56 GSPS at 8 bit) their small dynamic range is a severe issue for many cases. Furthermore, these platforms are very expensive and the related processing difficult, as such their integration has not started yet.

Multipurpose AMCs

The DAMC2 AMC board [13] is a multi-purpose FPGA hardware platform developed at DESY. It is the basis for systems used at DESY and EuXFEL for diagnostics, the Machine Protection System (MPS) [14] and the Photon Beam Loss Monitor (PBLM) [15]. At EuXFEL, the platform is used for the Clock and Control (C&C) project, an FPGA firmware responsible for the distribution of timing and veto information to 2D detectors [16]. A custom design RTM provides the connectivity to the Front End Modules (FEMs) of the detectors end through the use of a stacked RJ45 connector. One C&C RTM can support up to 16 FEMs which in turn supports a 1 megapixel detector, synchronizing the FEM operations with the overall facility timing and providing veto decisions.

FPGA DEVELOPMENT AND APPLICATIONS

FPGA projects at the European XFEL are developed mainly in VHDL and separated in two major entities: Board and Application (see Figure 2). The Board includes all code related to configure and monitor the Board features and also provides the Board interfaces (e.g. ADC/DAC, DDR2 controller, Clocks, etc.) to the Application module. The latter implements user algorithms and applications which may be Board specific. Improvements and further development on the board interfaces is performed by expert designers while not interfering with developments on the Application module. This fixed structure allows for easy porting and update of both board and application code. It provides an environment for firmware programming for standardized and future hardware.

FPGA projects and modules versions are managed in Gitlab repositories [17]. Source files must be saved within a specific structure which allows us to create generic scripts for the generation of firmware files, recreation of projects

under vendor FPGA tools, automatic versioning and continuous verification. Importing a module to a FPGA project is done using the git's submodule functionality, since there could be a requirement to use a specific module version or branch. This can can be related to compatibility, resource usage or even a custom configuration. Projects can be automatic updated in case a new module version is available.
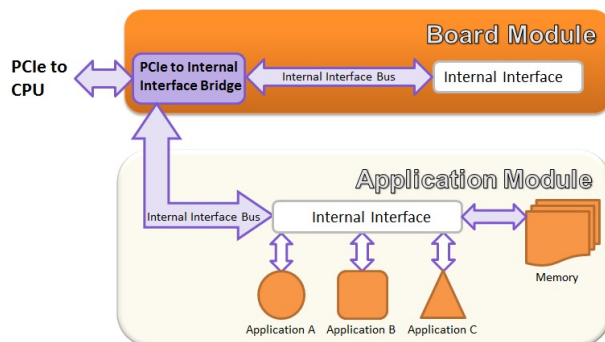

Figure 2: EuXFEL FPGA Projects Structure for in-house developed Firmware.

To define user registers and memories which can be access by PCIe devices or via Ethernet, our projects include a 32 bit wide internal bus based on the Internal Interface bus [18]. This bus protocol which includes a VHDL API package that eases register access and definition. Register properties such as access rights, type (internal or external bus register), bit size, data type (unsigned, signed), number of integer and fractional bits, memory length together with a brief description are defined in VHDL table types. Assignment of address and generation of internal bus registers are preform automatically during the compilation process. This allows register definition to be preformed at the hardware level. An XML file with all register information, including the assigned addresses, is available after compilation. The interfacing software library used in the European XFEL control system is able to interpret this file and provides a user friendly environment which allows users to communicate with the design on the FPGA.

In order to allow a universal identification of the installed hardware and firmware, we developed a standard register set concept, which is a predefined set of registers starting at address 0 and with a pointer to the next standard register set in the address space. In these registers crucial information about the type of hardware, functionality and versions is available even without access to the previously described XML files. This concept was further developed with different institutes and industry within a working group in PICMG and was released as a guide line called Standard Harware API (SHAPI) [19].

Data Processing and Reduction

FPGA algorithms for processing of digitizer data and reduction on the hardware are currently available and deployed in all AMCs. This data is provided together with the raw data and train information, allowing further systems to take
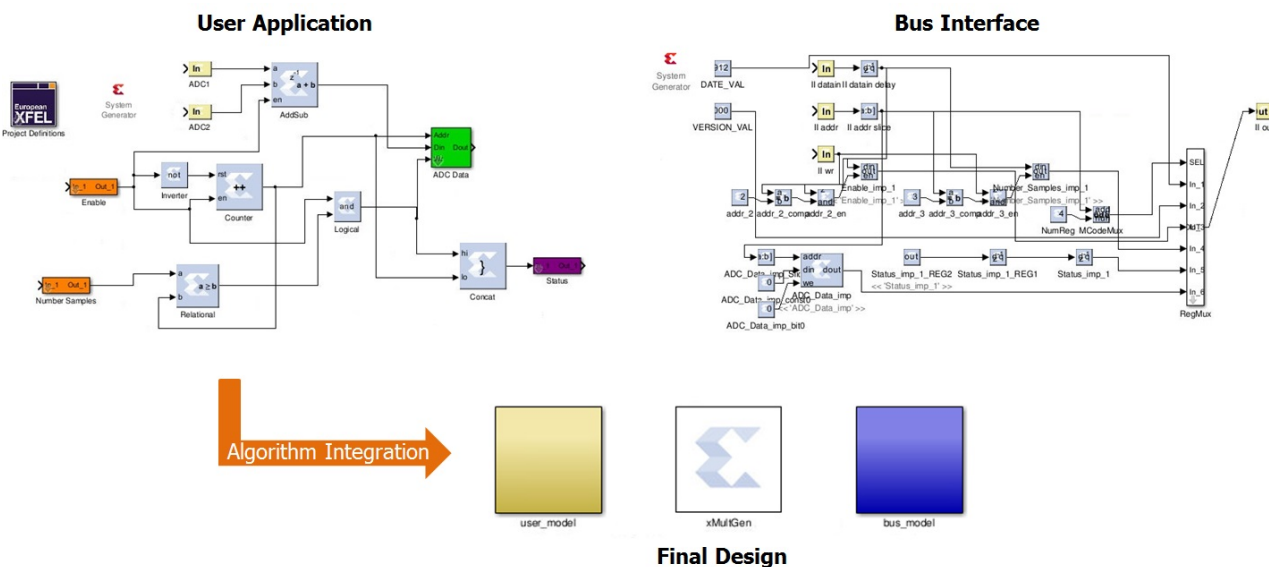
Figure 3: Example of a module design in XFEL's Simulink framework. The Bus Interface logic is generated during integration based on user defined registers. The bus model block includes the Bus Interface logic while a copy of the original algorithm is wrapped on the user model block.

faster decisions not only concerning the quality of the data, diagnostics and status of the beam and correlate it with different data sources. Algorithms include peak integration, peak (time) detection and zero suppression.

As mention before, information concerning train bunches is available to all devices that are able to receive the timing information, this includes the digitizers on the MicroTCA platforms, before the train arrives. All AMCs' FPGA firmware used by EuXFEL use a TimingInfo module that decodes the timing information, making it available for use in hardware applications. This information is used in a variety of ways for automatic data reduction and processing:

- enable data acquisition only for specific beam modes
- enable data acquisition according to the presence of bunches in the train, taking into account their destination, charge and/or presence of optical laser pulses
- automatic pulse integration according to the location, number and charge of bunches in the train
- start acquisition with a predefined time interval of the first bunch in the train
- configure the amount of raw data to acquire according to the time interval where only relevant bunches are present
- inform users of the number and location of bunches present in the train
- generate veto information according to the availability of bunches and/or optical laser pulses in the train. The user can choose to mask certain bunches for the acquisition of "dark" frames.

We have also adapted and integrated an open source TDC design [20] into the user space available in the ADQ412 firmware to improve the trigger resolution provided by the platform.

Simulink Environment

A high level FPGA framework based on Simulink is available at EuXFEL that allows users with no prior HDL knowledge to develop their algorithm modules which can be integrated in a FPGA project [21]. Xilinx libraries are available for the Simulink framework which include a considerable number of modules optimized for Xilinx FPGA boards [22]. The framework allows user defined registers and memories and to port applications to different projects. The register and memory definition are protocol agnostic during the development phase (see Figure 3). Only at the moment of integration the interface protocol (Internal Interface, AXI, etc.) must be specify, so the framework can generate the proper logic. The integration is transparent to the user.

The graphical programming language provided by Simulink allows for structured algorithms modules, reusability of existing blocks, while making debugging, simulation and development much faster. Integration with Matlab also allows for powerful test environments, namely the use of real data and integration of processing algorithms developed in other programming languages in simulation, time and frequency domain analysis as well as detailed signal analysis. From the FPGA project point of view, Simulink based designs are applications with their own memory in the bus protocol address space. In addition, algorithms and modules developed in VHDL are also available in the Simulink environment in the form of an EuXFEL Simulink library.

ON GOING AND FUTURE DEVELOPMENTS

The FPGA platforms presented have been integrated in EuXFEL before any user experiment, which began in late 2017. Since then, we have continuously updated the in-

house developed FPGA firmwares for all different so they are better aligned to what instrument colleagues and users require. The experience gathered from this feedback and work provides our team with clear directions on what to focus to address current and future challenges.

Concerning the MicroTCA platform, we are always interested in integrating new AMC solutions that may bring benefits to the user experiments. Updated versions of equipment presented here are already available from the vendors, such as the SIS8300 Kintex-Ultrascale. Migrating the developed firmware, algorithms and Simulink framework to these new FPGA architectures is a must. We are in close contact with DESY concerning the development of a successor for the Timing System and DAMC2 board. Working with external companies, we have approach N.A.T. Europe to update one of their AMC products to use newer FPGA architecture. This board allows direct communication with PLCs via the standardised industrial fieldbus EtherCAT [23], enabling direct communication between MicroTCA and PLC platforms and synchronize PLC actions with an external clock available in the AMC. EuXFEL is evaluating a prototype of this updated AMC, which uses a Zynq MPSoC and allows up to 8 connections to an EtherCAT network, and developing the main FPGA firmware (see Figure 4) [24].
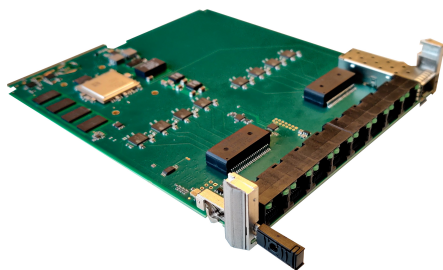

Figure 4: N.A.T.'s MicroTCA AMC EtherCAT solution (prototype).

Requests for more custom FPGA algorithms/solutions are expected to grow in the near future while also maintaining and updating the standard releases. We are taking steps on our FPGA development workflow to standardize validation and automatic generation of updated firmware versions. To take advantage of Gitlab's Continuous Integration, we are testing different UVM methodologies for VHDL code verification using only open source tools and frameworks. We are also considering Gitlab Runner as means to control firmware deployment.

More recently, institutes and companies are focused on providing libraries and frameworks that ease integration of FPGA platforms for data processing and acquisition. This is possible due to the higher abstraction tools provided by vendors that take care of complicated tasks such as scheduling of data transfer between CPU and FPGA, handling of custom data formats, kernels definition (FPGA modules for accelerating data computation on CPUs) and scaling solutions to multiple platforms and/or higher data volumes. These tools use HLS, openCL or graphical interfaces for development,

making them accessible to software developers. On an even higher abstraction level, the SYCL [25] open standard defines abstractions to enable heterogeneous device programming with several implementations already available.

We are interested in integrating platforms that take advantage on these tools for pre-processing and feature extraction of 2D detectors data. The ability of providing fast feedback to determine the data quality and/or to improve the setup is something that we aim to achieve. We started a collaboration project with Maxeler Technologies [26] for real-time processing on the raw data streams from 2D detectors. Maxeler uses OpenSPL [27] to program their FPGA based platforms. The current project integrates one of their solutions in a instrument for basic real-time calibration and visualization of recorded X-ray Images.

Machine Learning Applications

Machine learning (ML) is one of the significantly growing research fields, with applications in image processing, data analysis, data reduction, and many more. EuXFEL has dedicated great attention in improving the experimental process and optimizing the overall user experience, been proactive in looking at various methods for data optimization and automation, machine learning being one of them. Currently, there has been on-going efforts to realize the benefits of machine learning and deep learning within XFEL.

A research project was concluded this year which looked into state of the art tools for ML applications targeting FPGA platforms. Commercial and open source frameworks currently available focus on streamlining the process of hardware acceleration of a given ML application. These environments generate a High-Level synthesis code which can then be integrated to a FPGA platform. For architectures which already include both FPGAs and embedded processors, such as the Zynq family by AMD [28], the vendor frameworks can provide a complete firmware solution. Open source tools which are vendor agnostic, such as HLS4ML [29], allow for easy migration between different platforms.

As part of the research project, a workshop organized by PUNCH4NFDI [30] TA5 group and XFEL took place at DESY. The primary goal was the exchange about applications of machine learning on FPGAs, experiment specific challenges and solutions, as well as experiences with the different available frameworks. The presentations cover applications in particle physics, hadron physics, astrophysics and accelerator physics. The exchange will continue during monthly meetings and the wish for organizing a follow-up workshop next year has been expressed.

We intend to integrate FPGA based platforms for the acceleration software solutions developed internally by the Data Analysis group at EuXFEL, to achieving real-time results with latency in the nanosecond range.

SUMMARY

FPGA based hardware is at the center of real time processing, data acquisition for 1D detectors and timing distribution

solutions available in EuXFEL. MicroTCA is the main hardware platform used to host these boards, enabling high-speed communication between the cards, as well as distribution of clock and digital signals within the crate, and remote management and monitoring features. Our FPGA project structure and bus protocol provide a standard environment for firmware development and software integration. In-house developed FPGA applications are available for processing of raw data in hardware together with data reduction. We also provide a high-level FPGA programming framework that allows users to easily develop, simulate and integrate their algorithms into large FPGA projects.

Currently available libraries and frameworks, commercial and open source, ease the integration of newer FPGA architectures for acceleration of data processing and acquisition, while also offering a high degree of flexibility and scalability. These developments are key for current ML applications targeting FPGA platforms. We intended to get familiar with these tools and platforms to address the future challenges and requirements at EuXFEL.

ACKNOWLEDGEMENTS

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