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XILINX ZYNQ UltraScale+ USED AS EMBEDDED IOC FOR BPMs

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Abstract

PSI is using the Xilinx/AMD Zynq UltraScale+ (ZynqU+) MultiProcessing System-on-Chip (MPSoC) on different hardware platforms, ranging from VME and CompactPCI-Serial (CPCI-S) cards to customized platforms for high-volume applications like beam position monitors (BPMs) and magnet power supplies (PS).

The first ZynqU+ application at PSI was "DBPM3", a generic hardware platform for BPMs presently used for cavity BPMs in SwissFEL as well as button and stripline BPMs for the SLS 2.0 project. The DBPM3 platform has a digital backend with a ZynqU+, combined with an application-specific analog RF Front-End (RFFE) with integrated fast JESD204B ADCs.

This paper describes our experience with the application of ZynqU+ for EPICS IOCs of different applications at PSI, with focus on our first BPM applications. However, many of the topics and solutions discussed are also relevant and applicable for other applications.

INTRODUCTION

PSI contributed to the European XFEL by developing the BPM electronics and Intra-Bunch Train Feedback in collaboration with DESY and CEA/Saclay. The BPM electronics design for the European XFEL is based on the Xilinx/AMD Virtex5 FXT field programmable gate arrays (FPGAs) for low-level digital processing and control system interfacing, forming a hierarchy of FPGAs and CPUs. Shortly after PSI built the SwissFEL accelerator using the Xilinx/AMD 7-Series FPGAs (Artix-7 and Kintex-7), where PSI hardware and FPGA firmware concepts from the European XFEL were reused and adapted to the 7 Series FPGAs and SwissFEL requirements. When the Zynq UltraScale+ became available, we checked if the chip was suitable for new BPM hardware required for a 2nd SwissFEL soft X-ray beamline ("Athos") as well as for SLS 2.0, a major upgrade of the Swiss Light Source.

For the ZynqU+, we evaluated and verified that the ZynqU+ is able to integrate EPICS IOC, application specific real time processing, EVR triggering and other FPGA functionality all on a single chip. Moreover, we checked the performance of the IOC, compiled Petalinux, EPICS and implemented serial JESD204B ADC interfaces at 10 Gbit/s. After this successful evaluation, we chose the ZynqU+ for our future "DBPM3" hardware platform [1], combining functionalities of previously separated boards on one chip and printed circuit board (PCB), and thus reducing the number of connectors and potentially increasing the MTBF of our BPM systems.

DBPM3 PLATFORM

The DBPM3 unit is designed with stability, reliability and redundancy in mind. The analog electronics is separated from the digital backend. Only digital signals are routed through the connectors between front-end and back-end PCBs, using coplanar multi-pin high speed connectors without a backplane.

RF Front-End Boards

The RFFE boards of a DBPM3 system combine analog electronics and ADC on the same board, including an EEPROM for storage of calibration data. In order to minimize drift of the measurement data, the RFFE temperature is regulated by multiple heaters, combined with the fan speed regulation of DBPM3 19'' housing (see Fig. 1). The fans are supervised in EPICS, enabling early automated detection of fan degradation long before a fan breaks, thus improving system MTBF by avoiding urgent repairs.

Figure 1: DBPM3 unit.

Mechanics and Power Supply

The DBPM3 can incorporate various front-end board ("daughterboard") sizes, ranging from six single-width daughterboards with 50 mm x 300 mm size each to two triple-width boards with 152 mm x 300 mm size. Six daughterboard connectors are available on the back-end (one per single-width daughterboard), providing power, clocking, digital IO and serial multi-gigabit transceiver (MGT) links between JESD204 ADCs or DACs on the daughterboards and the ZynqU+ on the back-end board.

The power supply of the DBPM3 unit is redundant but does not support live insertion, since it is only one compact space-saving unit with a common mu-metal shield to minimize stray fields to the RFFEs. The power supply status is monitored by the EPICS alarm handler. If one of the two power supplies breaks, the 2nd one is able to power the complete unit, where the supply can then be replaced at the next maintenance day of the accelerator.

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Digital Back-End

The digital backend occupies a comparably small area in the DBPM3 unit. The V-shaped components at the bottom of Fig. 2 close to the Zynq UltraScale+ (black chip in the middle of the digital back-end) are the DDR4-SDRAM memories (including ECC), with one 72-bit DRAM connected to the Processor System (PS) and another to the Programmable Logic (PL) of the ZynqU+. Eight SFP+ transceivers at the front side of the DBPM3 unit are used for multi-gigabit serial communication with timing, control and feedback systems, using multimode or single-mode fiber optic transceivers up to 10 GBaud. Four SFP+ transceivers are connected to the PS, and four of them to the PL of the ZynqU+ MPSoC. The PS usually boots from network, where the PS software then loads and configures the PL.

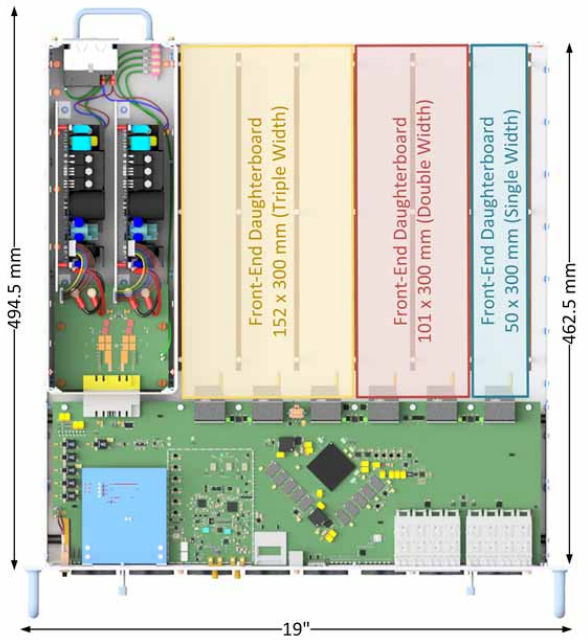

Figure 2: Top view of a DBPM3 unit (top cover removed), with redundant power supply (top left), support for up to six daughterboards with variable width (top right), and digital back-end with ZynqU+ (bottom).

Example Application: SwissFEL BPMs

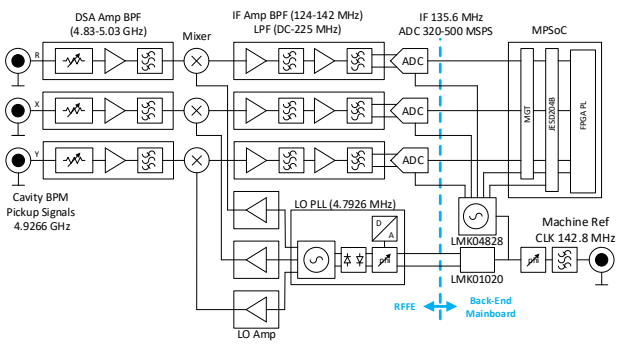

Figure 3: DBPM3-based cavity BPM electronics for SwissFEL.

While the DBPM3 unit is mainly targeting BPM applications, it is also suitable for other applications. The first application at PSI were SwissFEL cavity BPMs for the soft-X-Ray beamline Athos.

Figure 3 shows a simplified block diagram of the Athos DBPM3 BPM electronics. The RF front-end filters and amplifies the 4.9 GHz cavity BPM signals generated by the electron bunches, and down-converts them to an intermediate frequency (IF) of ~136 MHz that is then sampled by a 16-bit 500 MSample/s JESD204B ADC (also located on the RFFE). The ZynqU+ on the back-end retrieves the ADC signals at baud rates up to 10 Gbps. It also controls various components on the RFFE like attenuators, PLL and phase shifters, using several fast feedback loops to automate BPM operation and tuning for different operating conditions.

Since the ADC is part of the RFFE, there are no external cables between the analogue electronics and the digitizer (ADC) like in previous PSI BPM electronics generations. Purely digital signals are routed to the back end, hence the connectors and effects like contact aging and tolerances do no longer contribute to drift of the BPM measurement results.

SFP+ Transceivers and Protocols

The SFP+ transceivers of the DBPM3 unit that are connected to the PS MGTs are presently used for Gigabit Ethernet, but also support other standards like USB3.0, SATA, or PCIe (up to 6 GBaud). SFP+ transceivers connected to the PL MGTs are used for application-specific purposes (up to 10 GBaud), like feedback networks, or the embedded event receivers (EEVR) for SwissFEL and SLS timing/event systems. The EEVR, implemented in DBPM3 ZynqU+ PL by PSI, provides triggers synchronous to the machine and time stamp information for the control system. We also use the SFP+ transceivers to interconnect DBPM3 and other ZynqU+ systems, using e.g. an "AXI-AXI bridge" protocol developed at PSI that supports memory-mapped point-to-point connections between two ZynqU+ systems.

Since the SFPs are controlled by I2C multiplexers on the DBPM3 back-end, we need to guarantee that transactions are atomic and only one master is accessing them at a time. Otherwise the wrong SFP might be selected for read/write operations. Most of the configuration is static (SFP TX disable, rate select, etc.).

The DBPM3 unit uses mainly fiber optic SFP+ transceivers, using both multi-mode and single-mode fibers. The health status of SFP+ transceivers and fiber optic links (for network, event and feedback systems links) is monitored during operation via I2C, including the receive power of the fiber optic links, thus enabling early detection of transceiver degradation, or cable damage. Read/write access of the SFP+ transceivers is controlled by a firmware I2C component, keeping the requests sequentially consistent.

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Boot Process and Network Physical Layer

During the first boot phase of a DBPM3 unit after power-up, managed by U-Boot, we perform I2C-based configuration of DBPM3 back-end components like reference clock oscillators that may have application-dependent frequencies. The MAC address is read from an EEPROM, the Ethernet PHY ASIC is configured, control LEDs are set, and the SFP "TX disable" and "rate select" pins are set.

Figure 4 shows such a configuration of the SFP+ transceivers, using optical or electrical network connection. For PSI applications we prefer the fiber optic Ethernet connections, thus reducing ground loops and potential EMI problems. For tests in the lab, CAT6/7 network cables are also supported, employing SFP+ transceivers with RJ45 network connectors. The network connection type (CAT6/7 or optical) is selected by configuring U-Boot accordingly.

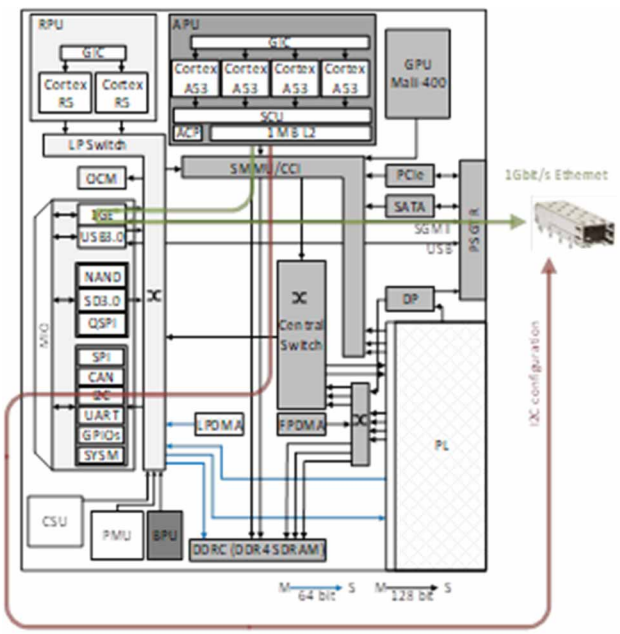

Figure 4: Configuring the SFP by I2C.

Memory and CPUs

The main memories of the DBPM3 are two sets of DDR4 SDRAMs. One memory is connected to the PL and the other one to the PS. This enables real-time streaming of ADC raw data to the PL DRAM without affecting the PS CPU performance that uses primarily the PS DRAM for code and data storage. Both the PL and PS DRAMs have 4 Gbyte size and are 72 bit wide, with 64 payload data bits plus eight ECC bits for error detection and correction.

The ZynqU+ PS has a 4-core 64-bit Cortex-A53 ARM CPU ("APU") used for Linux and EPICS IOC, and a 2-core 32-bit Cortex R5 ARM CPU ("RPU") for real-time DSP software (using RTOS or bare metal). Although one DRAM is connected to the PL and one to the (dedicated) PS I/O pins, both DRAMs can be accessed both by the PL and the PS by an on-board switch matrix. Thus, the PL is capable of streaming data not only to the PL but also to the PS DRAM. The latter enables easy data exchange with the EPICS control system running on the APU. Figure 5 shows a typical layout of the DBPM3 PS external SDRAM memory.

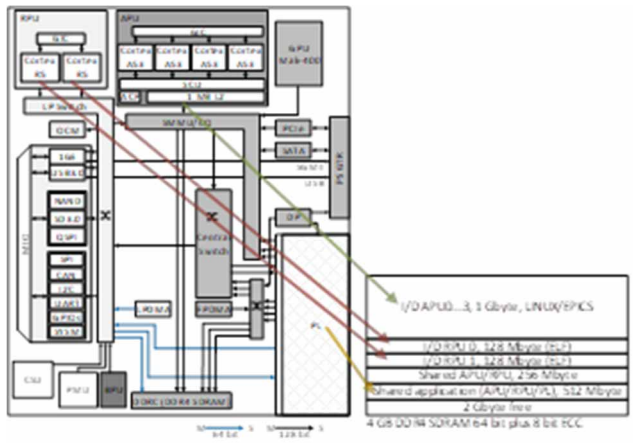

Figure 5: DBPM3 Main Memory Map for PS.

FIRMWARE/SOFTWARE DEVELOPMENT WITH VIVADO

The AMD/Xilinx Vivado software suite is used to develop the PL firmware. Most of the PSI PL components are based on the AXI4 bus standard, using several AXI4 masters (APU, RPU and DMA). Figure 6 shows the CPUs connected in parallel with the controls interface used by EPICS. The PS CPUs are interrupt controlled and able to access all devices on the AXI bus.

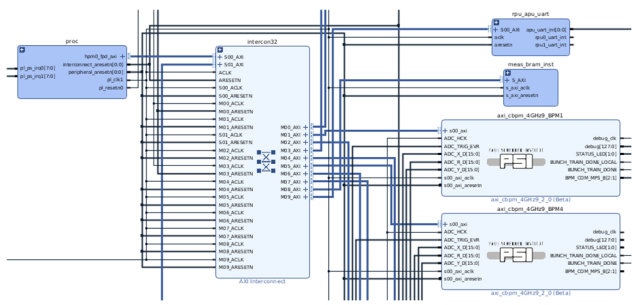

Figure 6: Block design.

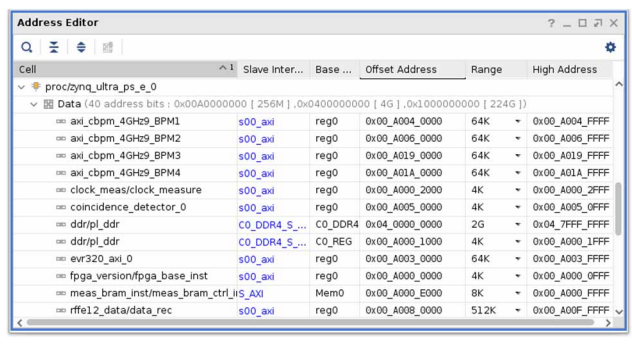

Figure 7: Address map.

The PS part uses AXI3 and the PL part uses AXI4 versions which differ in the size of burst transactions. Wider busses can be a work around to overcome this limitation. The AXI bus does not foresee a timeout, which may result in a deadlock if communication is broken after addressing phase of the AXI was acknowledged.

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Since our designs are based on the AXI4 bus, we can use Vivado to generate the memory map as shown in Fig. 7: Address Map. This map and additional information from the block diagram are exported for further use with SDK and EPICS configuration (base addresses and offsets for the components in the startup file and substitution file).

The code for the ZynqU+ software and firmware components is managed by git repositories, enabling efficient code sharing between different ZynqU+ projects. This reduces the testing effort and increases the development speed. Several instances of the same block can be instantiated and connected to the AXI interconnect. The documentation of the blocks can be attached such that with a mouse click the appropriate datasheet is displayed.

BOOT PROCESS

The Zynq UltraScale+ is configured by the mode pins to boot from the SD card (see Fig. 8). This will load the file "boot.bin" and in the next step start the second stage boot loader (U-Boot). The First Stage Boot Loader (FSBL) does the basic configuration of the system and U-Boot loads Linux onto the PS. U-Boot reads the environment file, on which the important information of the system is stored. This includes the name of the system, the configuration script for the hardware, boot server name, etc..

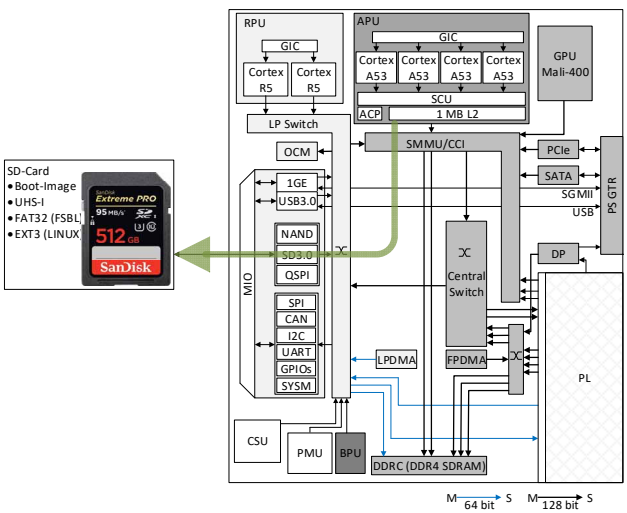

Figure 8: DBPM3 SD Card.

The SD card contains a file system that is readable and writable from the operating system on a PC. While ZynqU+ systems at PSI usually boot Linux, EPICS and PL firmware via network from a file server (see Fig. 9), it is also possible to store all related files directly on the SD card, including U-Boot and as well Linux, firmware, RPU software, drivers, EPICS startup files, substitution files and template files. In such a use case, the SD card is mounted in the Linux file system for simple upgrade of U-Boot and local applications. Such a fully autonomous functional system is convenient for operation and tests at facilities outside the PSI network, as well as for production and lab tests, where long-term independence of varying network, server and software environments is desired.

However, for the standard boot method at PSI, the DBPM3 unit loads software and firmware via Ethernet from a centralized server, using the second stage boot loader to load Linux from the file server into the PS SDRAM, where Linux runs on the APU. During the boot process of Linux, network drives of the boot servers are mounted. Linux then reads additional files from the server to finish the configuration of the DBPM3 unit:

- The firmware is loaded into the PL part of the Zynq UltraScale+
- The RPU software (bare metal or using FreeRTOS) is loaded in split mode (each RPU runs an own program code) or lock step mode (both RPU run the same program code) and executed in the SDRAM
- Finally, the EPICS configuration and drivers are loaded, and the EPICS IOC is started on the APU

The storage of PL firmware, RPU software and EPICS on a boot server helps keeping the system management effort and software distribution to a bare minimum. A simple file copy on the file server, followed by a reboot of the hardware, updates the system PL firmware, RPU software or EPICS configuration. However, as already mentioned above, the system can be as well operated as standalone unit and taken to another site without our PSI infrastructure. In this case all necessary files are stored on the SD card and ssh/telnet/UART can be used for remote low level access.

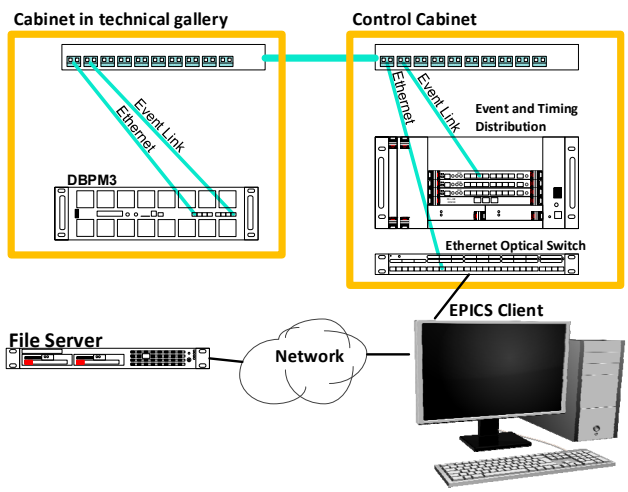

Figure 9: DBPM3 booting.

One of the last software modules loaded by Linux is an optional Xilinx Virtual Cable server. This server enables remote network connections of Xilinx Vivado on an office/lab PC to the Integrated Logic Analyzer or the Integrated Bus Analyzer on the ZynqU+, implemented in PL. This feature is convenient for efficient remote debugging of firmware and software by their developers.

EPICS IOC

The EPICS channels of PSI ZynqU+ systems are usually implemented using a generic driver/device support, where the memory offsets of the firmware I/O registers, on-chip and off-chip ZynqU+ RAM are contained in the INP/OUT

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fields of the EPICS channels, combined with the desired word size and other details. This approach enables use of the same driver/device support for different ZynqU+ systems, by adapting the EPICS template and substitution files accordingly, without having to write application-specific low-level IOC software. Figure 10 shows an example part of a template file, where EPICS uses the memory offsets to connect records to the desired PL components. The AXI Vivado component developer usually writes a matching EPICS template file for each PL component. This EPICS template file is then used in the substitution file, to connect to the respective instance in the firmware.

```
record(ao, "$(DEV)$(SYS)SMP-S1-2") {
  field(DESC, "Sampling timing S1.2")
  field(DTYP, "regDev")
  field(OUT,  "@$(BASE):$(PARAM_BASE)+0x0038: T=uint32 U=2000")
  field(LOPR, "0")
  field(HOPR, "255")
  field(EGU,  "clk cycles")
}

record(ai, "$(DEV)$(SYS)SMP-DONE") {
  field(DESC, "ADC sampling done")
  field(DTYP, "regDev")
  field(INP,  "@$(BASE):$(SMP_BASE_REG)+0x0004 T=uint32 V=$(IRQ)")
  field(SCAN, "I/O Intr")
  field(PRIO, "HIGH")
  field(FLNK, "$(DEV)$(SYS)SMP-IRQ-CHECK")
}
```

Figure 10: Two examples of PVs.

An important feature shown in the previous figure is hidden in the parameter "U=2000". This feature enables readback of output PVs at a regular rate, e.g. 2 s in the example shown above. This feature was originally implemented to operate two control systems in the European XFEL. One control system is DOOCS for accelerator operation by DESY, and the second one EPICS for remote maintenance by PSI. With this extension are were able to observe access of the system via DOOCS using EPICS and vice versa, e.g. for debugging purposes during the initial DOOCS software development (using existing and proven EPICS software). This feature is also useful in systems where low-level functions are accessible by more than one CPU. One example is a feedback running on a local CPUs that changes PL register set values (for example the attenuator on the RFFE board), where the periodic update of the EPICS output channel VAL field then enables the control room operator to see these changes immediately in EPICS GUIs. When the feedback is disabled, the operator can then set the attenuators manually, where the values in the GUIs are always up to date, without the need of duplicating channels and using a separate readback channel.

The "I/O Intr" in Fig. 10 shows how we implement interrupt driven scan rates. The PV "*SMP-DONE" is read when the interrupt with the interrupt vector set by $(IRQ) is issued. Then we read all the interrupt driven PVs in a forward chain. The Zynq UltraScale+ has 16 interrupt lines connected between PL and PS. We use the first eight interrupt lines for the APU-based EPICS triggering, and eight more interrupts for application specific interrupt routines in the RPU.

10G ETHERNET

In addition to the standard 1G Ethernet interface of the ZynqU+ PS that is used to boot the DBPM3 system and provide standard Linux/EPICS network access, we have implemented an additional 10G Ethernet interface in the PL of the ZynqU+, for optional high-volume streaming of measurement data e.g. during accelerator tests shifts. Since the PL is loaded after Linux has started, we use a Linux Device Tree Overlay to make functionality like 10G Ethernet known to Linux. The photo below shows two DBPM3 units connected to the same CISCO optical Ethernet switch, where we connected both the 1G PS and 10G PL interface.

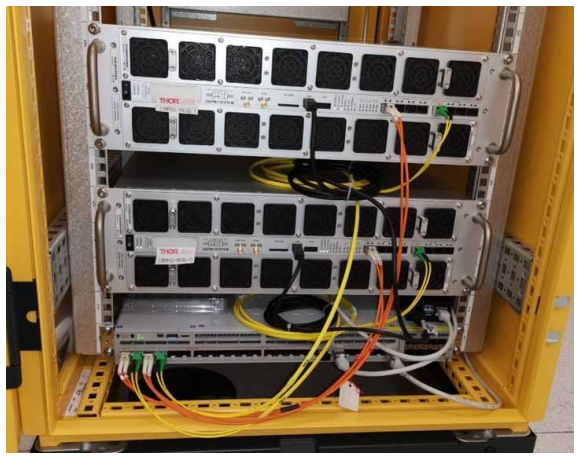

Figure 11: DBPM3 1 Gbit/s and 10 Gbit/s Ethernet.

```
root@DBPM3-MG82-1:/ioc/DBPM3-MG82-1# iperf3 -s
-----------------------------------------------------------
Server listening on 5201 (test #1)
-----------------------------------------------------------
Accepted connection from 129.129.158.97, port 35272
[  5] local 10.10.10.28 port 5201 connected to 10.10.10.29 port 45672
[ ID] Interval           Transfer     Bitrate
[  5]   0.00-1.00   sec   390 MBytes  3.27 Gbits/sec
[  5]   1.00-2.00   sec   397 MBytes  3.33 Gbits/sec
[  5]   2.00-3.00   sec   396 MBytes  3.32 Gbits/sec
[  5]   3.00-4.00   sec   395 MBytes  3.32 Gbits/sec
[  5]   4.00-5.00   sec   395 MBytes  3.31 Gbits/sec
[  5]   5.00-6.00   sec   395 MBytes  3.32 Gbits/sec
[  5]   6.00-7.00   sec   397 MBytes  3.33 Gbits/sec
[  5]   7.00-8.00   sec   395 MBytes  3.31 Gbits/sec
[  5]   8.00-9.00   sec   395 MBytes  3.32 Gbits/sec
[  5]   9.00-10.00  sec   397 MBytes  3.33 Gbits/sec
[  5]  10.00-10.00  sec   690 KBytes  3.11 Gbits/sec
- - - - - - - - - - - - - - - - - - - - - - - - -
[ ID] Interval           Transfer     Bitrate
[  5]   0.00-10.00  sec  3.86 GBytes  3.32 Gbits/sec                  receiver
-----------------------------------------------------------
Server listening on 5201 (test #2)
-----------------------------------------------------------
```

Figure 12: Performance of the 10 Gbit/s Ethernet.

During first tests of the implemented 10 G interface, the data throughput was higher compared to 1G, but not as high as expected. The cause appears to be the CPU/Linux interrupt rate of the 10G Ethernet MAC. Enabling Jumbo frames on the Zynq and the Ethernet Switch has increased the data rate, but the measured data throughput of 3.3 Gbit/s with our present test setup (see Figs. 11 and 12) is still significantly below the theoretical maximum.

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APPLICATIONS

SwissFEL BPMs

The EPICS interface for typical ZynqU+ applications at PSI include a smaller number of channels used by control room operators and physicists, plus a larger number of channels for the developers and system experts. While operators are mainly interested in properties like beam positions, charge and arrival time calculated by the ZynqU+ of a BPM system, system experts and developers also need read and write access to EPICS channels for intermediate results, system calibration and tuning, health monitoring, and efficient diagnostics of abnormal conditions and hardware failures.

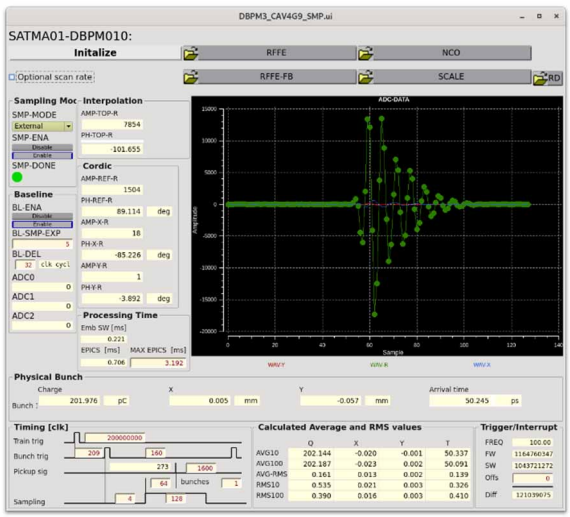

Figure 13: SwissFEL 4.9 GHz Cavity BPM GUI.

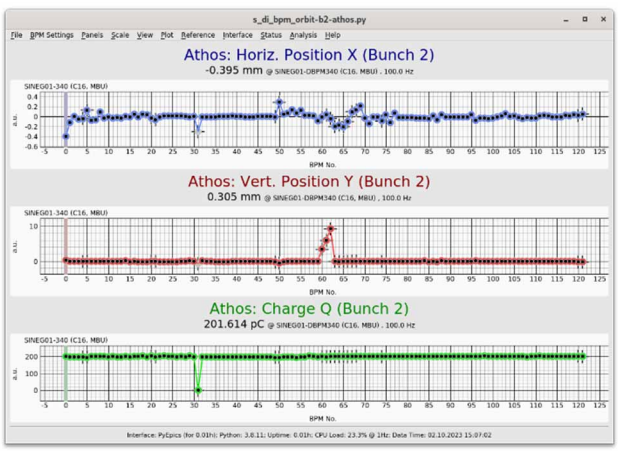

Figure 14: SwissFEL overview BPM GUI.

The DBPM3 systems at SwissFEL measure beam positions at a rate of up to 100 Hz. Each bunch in SwissFEL has a unique number ("PulseID"), serving as a unique time stamp, that is distributed by the SwissFEL timing/event system and received by the DBPM3 via the EEVR of the ZynqU+. The ZynqU+ is thus able to time stamp its measurement data directly on low-level, before forwarding the data to the EPICS IOC and beam-synchronous archiving system.

While this archiving is done at the full 100 Hz data rate, graphical user interfaces in the control room usually display the data at a lower rate of typ. 5 Hz, where we use two sets of EPICS channels for 100 Hz data and decimated data for GUIs.

Some GUIs like the one in Fig. 13 show data for a single BPM, while other GUIs show data of many or all BPMs, like the global SwissFEL orbit and charge display in Fig. 14. In order to make sure that the decimated beam position and charge data for different BPMs originates from the same bunch, we use a suitable modulo of the PulseID to trigger the update of the respective EPICS channels.

SLS 2.0 Feedbacks

Further applications of ZynqU+ MPSoC at PSI include the new fast orbit feedback (FOFB) for SLS 2.0, a major upgrade of the SLS ("1.0") with a new storage ring that will be commissioned in 2025. The SLS 2.0 multibunch feedback will be based on Xilinx RF Systems-on-Chip (RFSoC), which is basically a ZynqU+ MPSoC combined with several high-speed ADCs and DACs on the same chip. Prototypes of these systems have been successfully tested with beam at SLS before the machine was shut down 9/2023 and the installation of SLS 2.0 has started.

For tests of the SLS 2.0 FOFB prototype system at SLS 1.0, we interfaced a new centralized ZynqU+ based feedback engine to the existing old VME-based SLS 1.0 magnet power supply controller boards and BPM hardware that are all based on VME, using an additional "GPAC3" FPGA board in the VME crate to interface BPMs and magnet PS to the new feedback engine via MGT fiber optic links. With these links, we connected the AXI on-chip bus of the GPAC3 7-series FPGAs with the ZynqU+ on the feedback engine, using a multi-master AXI-AXI fiber optic protocol developed at PSI. This enables the ZynqU+ to retrieve the data of the old SLS 1.0 BPMs, and to write the set values of the orbit corrector magnet PS calculated by the ZynqU+ based FOFB engine back to the VME systems. With this setup, we were able to close the FOFB loop and stabilize the SLS 1.0 beam with the new prototype SLS 2.0 FOFB, using preliminary hardware, firmware and software solutions that will be replaced by the final SLS 2.0 versions presently being developed.

Other Applications

Additional ZynqU+ applications at PSI include SLS 2.0 magnet power supplies, CPCI-S boards for general applications, as well as upgrade of older SwissFEL BPM electronics. This electronics does not yet have an on-board EPICS IOC, but is so far using external VMEbus IOCs connected to the electronics via multi-gigabit fiber optic links. These VMEbus IOCs will be replaced by a ZynqU+ IOC located on a commercial SoM (system-on-module). This SoM can be plugged onto the FPGA board of the old BPM system, where a suitable mezzanine connector had already been foreseen for exactly this purpose.

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SUMMARY AND OUTLOOK

PSI has successfully deployed ZynqU+ MPSoCs for SwissFEL BPMs that are now in 24/7 user operation, including embedded event receivers and EPICS IOC running on the ZynqU+ of the generic "DBPM3" back-end solution developed at PSI. The next DBPM3 applications at PSI are at SLS 2.0, where an electronics prototype has been successfully tested [2], as well as the BPM upgrade of the high intensity proton accelerator HIPA, where the development of a HIPA-specific DBPM3 RFFE has just started.

After pioneering ZynqU+ at PSI for BPM systems, several other ZynqU+ applications and hardware solutions have been developed or are under development by various PSI groups.

CONCLUSION

The Zynq UltraScale+ has become the de-factor standard for new embedded measurement and feedback systems at PSI, with a growing number of applications. Compared to the previous VMEbus standard at PSI where EPICS IOC and FPGA were located on different chips or even different boards, ZynqU+ MPSoC solutions with integrated IOC may increase the system complexity on the software/firmware side, but the user is rewarded with more functionality and higher performance. The tighter integration of several hardware, firmware and software components on a single chip with its high-speed on-chip AXI interconnect not only boosts the system performance, but also simplifies the hardware development, increases firmware/software synergies between applications, and provides more independence of crate and board standards.

So far, most applications at PSI use the APU of the ZynqU+ to run Linux and EPICS IOC, and the RPU as well as PL for real-time signal processing. For development and operation of the systems, the Xilinx Virtual Cable is a valuable and efficient remote debugging tool to speed up development and system diagnostics by efficiently tracking down problems.

Last but not least, network booting of the firmware, RPU software, Linux and EPICS from centralized boot servers simplified version management of a growing number of systems.

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