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DYNAMICAL MODELLING VALIDATION AND CONTROL DEVELOPMENT FOR THE NEW HIGH-DYNAMIC DOUBLE-CRYSTAL MONOCHROMATOR (HD-DCM-Lite) FOR SIRIUS/LNLS*

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Abstract

Two new High-Dynamic Double-Crystal Monochromators (HD-DCM-Lite) are under installation in Sirius/LNLS for the new beamlines QUATI (quick-EXAFS) and SAPUCAIA (SAXS), which requires high in-position stability (5 nrad RMS in terms of pitch) whereas QUATI's DCM demands the ability to perform quick sinusoidal scans in frequencies, for example 15 Hz at 4 mrad peak-to-peak amplitude. Therefore, this equipment aims to figure as an unparalleled bridge between slow step-scan DCMs, and channel-cut quick-EXAFS monochromators. In the previous conference, the dynamical modelling of HD-DCM-Lite was presented, indicating the expected performance to achieve QUATI and SAPUCAIA requirements. In this work, the offline validation of the dynamical modelling is shown, comparing to the solutions achieved for the previous version of LNLS HD-DCMs. This work also presents the hardware-based control architecture development, discussing the loop shaping technique and upgrades in the system, such as the increase of the position resolution, synchronization of the rotary stages, and FPGA code optimization. Furthermore, it describes how the motion controller was developed, given the high-performance motion control, such as complex control algorithm in parallel with a minimal jitter and the expectations for the beamlines commissioning regarding detector and undulator synchronization.

INTRODUCTION

Two new High-Dynamic Double-Crystal Monochromators (HD-DCM-Lite) are currently undergoing the offline commissioning at Sirius [1]. In this context, the dynamic behavior of all components that involve motion is being collected experimentally and validated together with the model provided by the mechanical design. The controller for each degree of freedom is also being designed. In addition to that, new mechatronic tools to control such unprecedented systems are being developed by the LNLS team members. This development is important because the HD-DCM-Lite is an engineering challenge, and the development of systems to solve problems related to precision and stability is essential for a laboratory which aims to be innovative and ambitious in technology.

The identification and control system present in this work are based on frequency domain analysis and the operation is based on a NI CompactRIO (cRIO) 9049 [2] – so the mechatronic tools that will be shown require high performance programming in terms of resources and timing optimization for high-speed calculations in single precision, on a hardware-based platform. This work presents the results of the offline commissioning and perspectives for the online commissioning.

ARCHITECTURE

Cartesian Convention Guideline

In the next sections of this paper, the actuators and sensors that belong to HD-DCM-Lite will be explained. Each one of them controls a degree of freedom which is aligned with the standard axes of the laboratory. The goniometers (rotary stages) that control the 1st crystal – and consequently the Bragg angle (θ) – have a degree of freedom that is aligned with the x axis of the laboratory. The Short-Stroke, responsible for maintaining the beam at the same height H after meeting the 2nd crystal, controls three degrees of freedom: GAP (or gap, a translation aligned with y' axis), PTC (or pitch, a rotation aligned with the x axis) and RLL (or roll, a rotation aligned with the z' axis). These orientations are shown in Fig. 1.

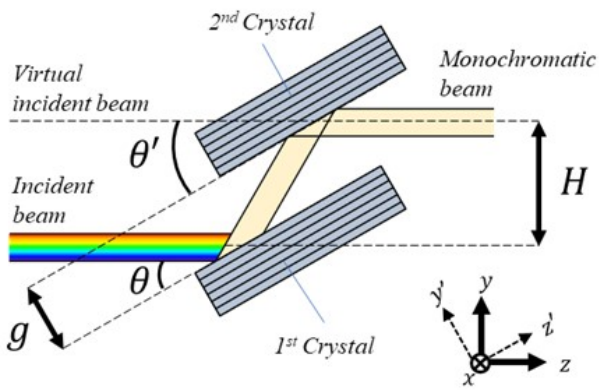

Figure 1: Cartesian convention guideline for the monochromator.

Goniometers

As seen in [3], the goniometers of HD-DCM-Lite are mechanically connected. To achieve scan results closer to the expectations demanded by the quick-EXAFS experiments, a gantry closed loop will be designed in the next few months. For the preliminary results and offline commissioning, the goniometers are controlled individually – each one with the respective controller. The goniometers – Aerotech APR260-DR180 for ultra-high vacuum [4] – are brushless actuators,

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so they demand three currents with 120 degrees of phase be-tween each one. The current controller is a Varedan Stand-Alone LA415 [5]. Figure 2 shows the implemented architecture for the offline validations.

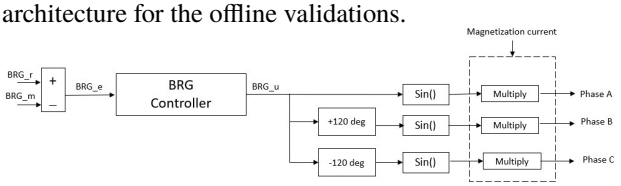

Figure 2: General control architecture for individual goniometer.

The code architecture that runs on the cRIO 9049 FPGA is based on the following items:

- BRG_m is the measured value of the Bragg angle, provided by the goniometer, in degrees. The digital signals are read by a NI-9753 module (digital I/O, 10 MHz sample rate) [6] and converted to values in degrees.
- BRG_r is the reference, or desired value, for the Bragg angle, in degrees.
- BRG_e is the position error for the Bragg angle, in degrees.
- BRG_u is the control effort to feed the commutation architecture, and it can be interpreted as the amount of magnetization rotates inside the brushless motor.

Short-Stroke

The general architecture developed for Short-Stroke is based on individual controllers for each degree of freedom: gap (GAP), pitch (PTC) and roll (RLL) [7]. The individual controllers were chosen because the system identification shows that the degrees of freedom are close to an uncoupled condition. Then the whole system can be modelled as a SISO mechanism, in which the efforts are a translational force to control the GAP and two momentums to control the PTC and the RLL. In other words, the low crosstalk between the degrees of freedom allows to build the architecture shown in Fig. 3 – not considering the disturbances and noises and showing only the variables that appear in the low-level code, running inside FPGA.

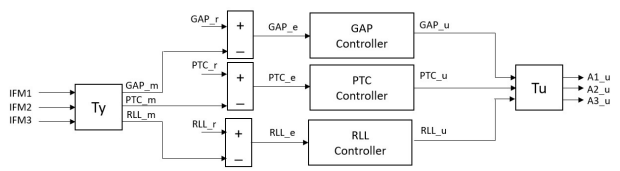

Figure 3: General control architecture for Short-Stroke.

The blocks identified as Ty and Tu represent homogeneous transformations (or kinematics). As the Short-Stroke is a tripod with three controlled degrees of freedom (one translation and two rotations) and the actuators only provide translations, then the following matrix calculations must be done:

$$\begin{bmatrix} GAP\_m \\ PTC\_m \\ RLL_m \end{bmatrix} = \frac{1}{3r_{\text{sens}}} \begin{bmatrix} r_{\text{sens}} & r_{\text{sens}} & r_{\text{sens}} \\ 2 & -1 & -1 \\ 0 & \sqrt{3} & -\sqrt{3} \end{bmatrix} \begin{bmatrix} IFM1 \\ IFM2 \\ IFM3 \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} A1\_u \\ A2\_u \\ A3\_u \end{bmatrix} = \frac{1}{3r_{act}} \begin{bmatrix} r_{act} & 2 & 0 \\ r_{act} & -1 & \sqrt{3} \\ r_{act} & -1 & -\sqrt{3} \end{bmatrix} \begin{bmatrix} GAP\_u \\ RLL\_u \\ PTC\_u \end{bmatrix} \quad (2)$$

In which $r_{\text{sens}} = r_{\text{act}} = 0.1$ m are the radii of the circumferences defined by the three sensors and three actuators respectively. The code architecture that runs on the cRIO 9049 FPGA is based on the following items:

- IFM1, IFM2 and IFM3: raw measurements provided by interferometers (SmarAct: model F04), with PicoScale driver to encode the signal into digital [8]. They're aligned with the actuators. The digital signals are read by a NI-9753 module (digital I/O, 10 MHz sample rate) and converted to values in meters.
- GAP_m, PTC_m and RLL_m are the measured values of the degrees of freedom that belong to Short-Stroke – in meters, radians and radians, respectively.
- GAP_r, PTC_r and RLL_r are the references, or desired values, of the degrees of freedom that belong to Short-Stroke – in meters, radians, and radians, respectively.
- GAP_e, PTC_e and RLL_e are the position errors of the degrees of freedom that belong to Short-Stroke – in meters, radians and radians, respectively.
- GAP_u, PTC_u and RLL_u are the control efforts of the degrees of freedom that belong to Short-Stroke – in Newtons, Newton-meters and Newton-meters, respectively.
- A1_u, A2_u and A3_u are the efforts to be applied in the actuators (voice-coils AVM40-HF-6.5, by Akribis [9]) – all in Newtons. Following the datasheets, these values need to be converted to Voltage to be sent from a NI-9269 analog output module [10] to the current drivers (TA105 by Trust Automation [11]).

SYSTEM IDENTIFICATION (SHORT-STROKE)

As the monochromators in Sirius beamlines are one of the most critical systems and directly influence the quality of the experiments, a system identification shall be done for all degrees of freedom in order to design a controller able to reach the targets of the project. This section explains the system identification procedures, from signal generation to the solution of assembly problems by looking at the frequency-response graphs.

The system identification applied in the Short-Stroke of HD-DCM-Lite is analogous to previous HD-DCMs implemented at Sirius, concerning the conception and how the efforts are turned into motion. The main difference is the application of the excitation signals and feedback synchronized acquisition using the final hardware (cRIO 9049), instead of a prototyping equipment (SpeedGoat) [12], since plant identification and validation during assembly phases are crucial for reliability and diagnostics, indeed it provides significant time saving. Also allows a faster validation of different signals and resulting controllers from identified plants. After

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the excitation and acquisition, the data is imported to MATLAB to be postprocessed – this includes the process from the Frequency-Response graphs building using fast Fourier transforms to the controller design using the loop shaping method, later explained in this paper.

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Stimulus Signals

The excitation signals are based on a multi sine signal generation – this one is a sum of several components in frequency domain. The signal is divided in 20 periods – in which each period corresponds to 1 second – with equal data. In the first and last 2 seconds, the general amplitude grows through a Tukey window, and the data used for system identification is contained in the 16 seconds, in the middle of the experiment. Each period of these 16 seconds brings a Frequency-Response data from effort to degrees of freedom, and then the final Bode diagram is a simple average between each identification period. Also, the frequencies that belong to the multi sine signal follow a Schroeder phasing. All these elements bring significant improvements on the signal-noise ratio and to the repeatability of the components that comprise the general dynamic behavior of the system.

In the cRIO 9049, the excitation signals are generat-ed in the RT code and passed to FPGA through FIFOs [13], as this stream can occur in high rates without overloading the buffers.

Table 1 shows the characteristics of the excitation data for each degree of freedom. The multi sine signal based on Schroeder phasing has a minimum frequency (Fmin), a delta frequency (Fdelta) and a maximum frequency (Fmax). The excitation signal is also modulated (Mod). It is also important to note the maximum frequency that can be identified is 10 kHz, as it's equal to the loop rate – 20 kHz – divided by two, corresponding to the Nyquist frequency.

Table 1: Characteristics of Excitation Data for Short-Stroke System Identification

From	Fmin	Fdelta	Fmax	Mod
GAP_u	1 Hz	1 Hz	10 kHz	0.5 N
PTC_u	1 Hz	1 Hz	10 kHz	0.025 N·m
RLL_u	1 Hz	1 Hz	10 kHz	0.015 N·m

Results: Frequency-Response and Crosstalk

Figure 4 shows the Frequency-Response for all 9 systems that belong to Short-Stroke. In this condition, the goniometers (BRG) are positioned in 30° (equilibrium point of the balance-mass), and the mechanism is inside a vacuum vessel. Figure 5 shows the crosstalk between the degrees of freedom. This is important to demonstrate that the whole system can be interpreted as a set of 3 individual systems (from GAP_u to GAP_m, from PTC_u to PTC_m and from RLL_u to RLL_m), representing a SISO construction. In these systems, the relative gain array (RGA) must be close to 1 [14]. In order to interpret it as a SISO, the RGA of other degrees of freedom must be close to 0. For example: the RGA of system from GAP_u to GAP_m must be close to 1, while from GAP_u to PTC_m or to RLL_m must be close to 0.

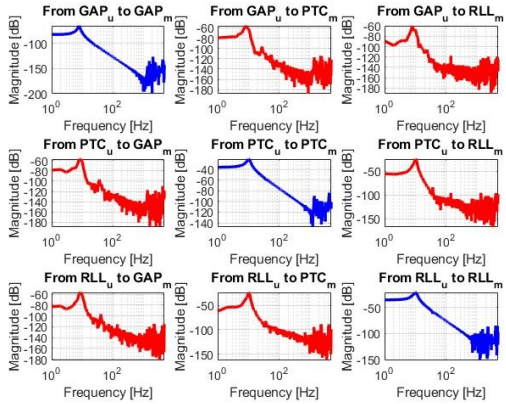

Figure 4: Frequency-Response for Short-Stroke.

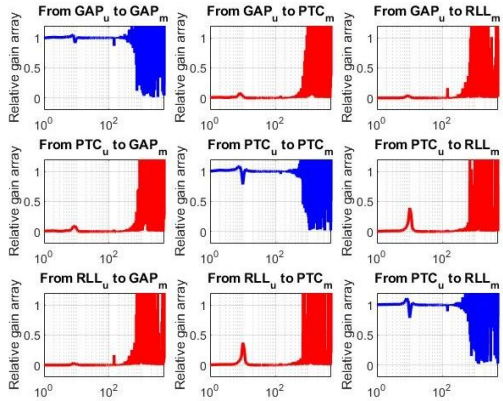

Figure 5: Crosstalk for Short-Stroke.

By observing the crosstalk plot for Short-Stroke, the main conclusion is that it can be approximated to a SISO system and the individual controllers can be applied – matching the mechanical design and constructions.

Comparison with Model

A very important step after identifying the plant experimentally is to compare the results to the model, discussed in previous papers about HD-DCM-Lite. Figure 6 shows the comparisons using the Bode diagrams of the identified plants and the model obtained during the mechanical design. By observing the unified plots (identified plants and the dynamical modelling), the conclusion is that the mechanical assembly follows the design concerning the dynamical behavior. Also, the observed results during the offline commissioning were good and matched the beamline expectations in terms of in-position error (RMS). This is essential for a good offline commissioning. The results will be shown in the next few sections.

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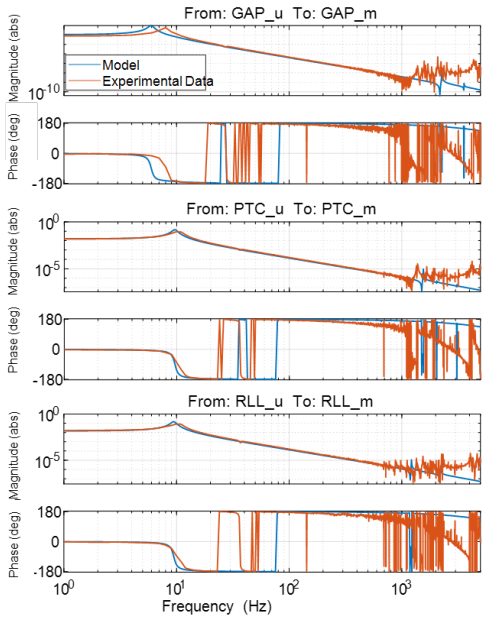

Figure 6: Bode diagram for Short-Stroke: model versus experimental.

Problems Fixed During Assembly, Realized by System Identification

It is important to emphasize that some problems were realized after the first system identification procedures done for HD-DCM-Lite. A relevant one was the re-work on the cooling manifold. Figure 7 shows the plants before and after that. It is visible that the re-work brought a dynamical behavior that has a better perspective on controller design, as some components in high frequencies disappeared.

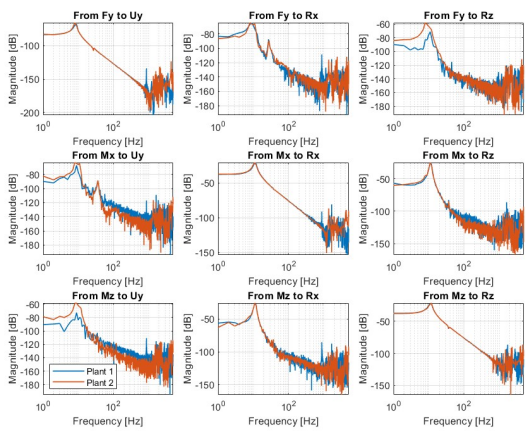

Figure 7: Identified plants during the manifold investigation. Plant 1: before the re-work. Plant 2: after the re-work.

CONTROLLER DESIGN (SHORT-STROKE)

In this section, the controller design for Short-Stroke is detailed. It is important to emphasize that the design applies the loop shaping method [15], using the identified plants shown in the last section. This method was chosen due to the good results presented in previous HD-DCMs in terms of RMS error and stability. Also, following the same guidelines, the controllers were designed in continuous time domain, and then discretized using a sample time of 50 microseconds (as the servo loop runs at 20 kHz) with Tustin approximation. This is necessary, as the FPGA runs the controllers using discretized transfer functions – this architecture is detailed in the next section.

The typical controller blocks that are designed to control HD-DCMs at Sirius are proportional gains, integrators, lead-lags, 2nd order low-pass filters and notches. Their formats are the following (in continuous time domain, to be discretized before embedded into FPGA):

$$C_{\text{prop}}(s) = K_p \tag{3}$$

$$C_{\text{lead-lag}}(s) = \frac{s + Z_{ll}}{s + P_{ll}} \tag{4}$$

$$C_{\text{int}}(s) = \frac{s + Z_{\text{int}}}{s} \tag{5}$$

$$C_{\text{low-pass}}(s) = \frac{1}{s^2 + 2\xi\omega_c s + \omega_c^2} \tag{6}$$

$$C_{\text{notch}}(s) = \frac{s^2 + 2\xi_z\omega_c s + \omega_c^2}{s^2 + 2\xi_p\omega_c s + \omega_c^2} \tag{7}$$

The designed controllers – in continuous time domain – for each degree of freedom that belongs to Short-Stroke are described in the Table 2.

Table 2: Designed Controllers for Short-Stroke, in Continuous Time Domain

Controller component	**GAP**	**PTC**	**RLL**
Proportional gain	2400000	10900	7000
Lead-lag zero	50 Hz	65 Hz	900 Hz
Lead-lag pole	1100 Hz	1500 Hz	900 Hz
1st integrator zero	1 Hz	2 Hz	2 Hz
2nd integrator zero	1 Hz	3 Hz	2 Hz
2nd order low pass filter freq.	1000 Hz	1300 Hz	800 Hz
2nd order low pass filter damp	0.2	0.15	0.2
1st notch frequency	2135 Hz	1400 Hz	885 Hz
1st notch zero damp	0.01	0.01	0.02
1st notch pole damp	0.1	0.2	0.2
2nd notch frequency	1600 Hz	1700 Hz	700 Hz
2nd notch zero damp	0.02	0.02	0.05
2nd notch pole damp	0.1	0.2	0.1
3rd notch frequency	1400 Hz	2550 Hz	N/A
3rd notch zero freq. damp	0.02	0.05	N/A
3rd notch zero freq. damp	0.1	0.2	N/A

By having the designed controllers and the Frequency-Response data of the system, it is possible to analyze the expected performance in terms of bandwidth and margins.

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Table 3: Performance After Designing Controllers via Loop Shaping Method: Target and Reached

Performance parameter	Target	GAP	PTC	RLL
Bandwidth	200 Hz	226 Hz	287 Hz	173 Hz
Modulus margin	<10 dB	8.8 dB	8.9 dB	8.8 dB
Phase margin	>30°	35.96°	31.73°	34.02°
Gain margin	>6 dB	4.5 dB	4.1 dB	5.8 dB

Table 3 shows the comparison between the reached performances and the targets defined during the project conception.

It is important to note that the bandwidth, the phase margin and the gain margin are provided by the Bode diagram of the open-loop system (plant and controller in series). Figure 8 shows the plot for all systems involved in Short-Stroke control. By having the open-loop diagram, it is possible to obtain the expected Nyquist diagram for this condition. Figure 9 shows the corresponding Nyquist diagram and the circles that represent the modulus margins for three cases: 6 dB, 8 dB and 10 dB.The diagrams shown in this section, provided by the identified plant of the dynamic system, together with the designed controllers, indicate the system will be stabilized when submitted to a closed-loop condition, in such a way that the noises are not expected to be amplified and turned into a problem for the operation of HD-DCM-Lite. Also, the high bandwidth and positive margins (phase, gain and modulus) indicate it as well. After submitting the Short-Stroke to the closed-loop condition in the offline commissioning, the results matched the expectations defined by the mechanical design, in terms of in-position RMS error:

- For GAP: less than 1 nm (RMS).
- For PTC: less than 7 nrad (RMS).
- For RLL: less than 8 nrad (RMS).

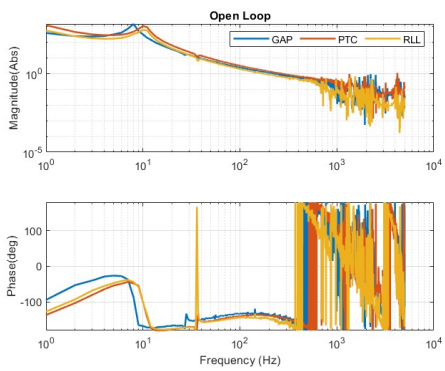

Figure 8: System + controller in open-loop.

The mentioned results were acquired in a condition in which the goniometers were kept stopped with an error equal to 1 count peak-to-peak (equivalent to approximately 191 nrad). These results are essential for the good operation of HD-DCM-Lite, specially at SAPUCAIA beamline (SAXS).

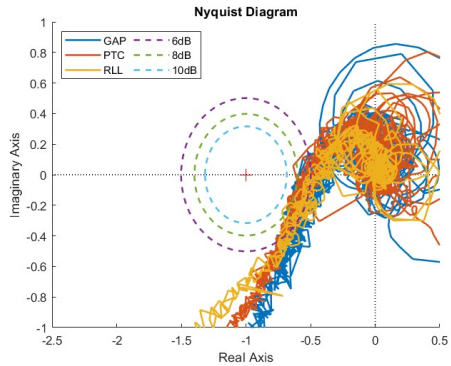

Figure 9: Nyquist diagram of the controlled systems.

SYSTEM IDENTIFICATION (GONIOMETERS)

In the same way as the Short-Stroke case, the goniometers shall be identified so that a stabilizing controller in closed-loop can be designed. The architecture described in this paper – to accomplish with the offline commissioning – takes the electrical phase as the control effort to move the system. The identification process is analogous to what has been described for Short-Stroke, but the commutation of the effort to be sent to the goniometer follows the architecture described above. The multi sine characteristics – with Schroeder phasing and modulation by Tukey windowing – follows the values present on Table 4.

Table 4: Excitation Signal for System Identification on Individual Goniometer

From	Fmin	Fdelta	Fmax	Mod
BRG_u	1 Hz	1 Hz	2500 Hz	1°

It is important to emphasize that the goniometers' loop rate is equal to 5 kHz – differently from Short-Stroke, which was fixed up to 20 kHz. In the code dedicated to HD-DCM-Lite, the loops running inside FPGA are different for Short-Stroke and for goniometers. In previous versions of HD-DCM, the loop is the same. The division in two different loops brought a better code modularization and error handling. Other important factor is that, in the actual conjuncture of the project, the goniometers are controlled individually – and posteriorly they will be in a gantry controller. So, the excitation is also individual. The result for an individual identification (in this specific case, exciting the second goniometer and leaving the first one disabled) is present on Fig. 10 (magnitude) and Fig. 11 (phase).

By looking at the goniometers identifications at different magnetization current conditions, it is possible to visualize that the application of 2 A into the commutation architecture brings a system with better control perspectives due to the DC gain before the resonance. So, for the offline commissioning, the magnetization current was fixed in 2 A.

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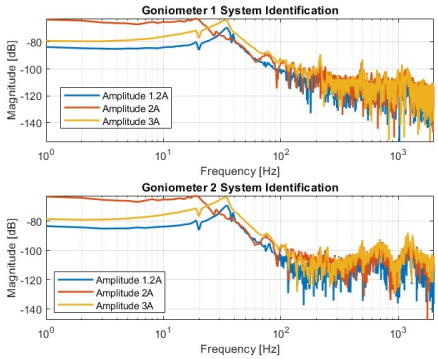

Figure 10: System identification for goniometers (magnitude).

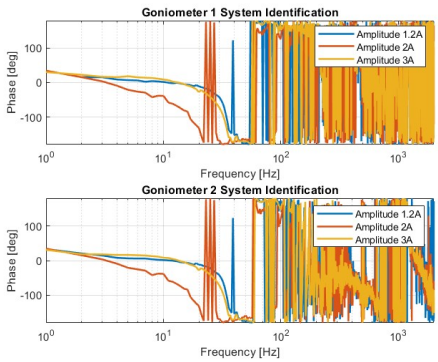

Figure 11: System identification for goniometers (phase).

CONTROLLER DESIGN (GONIOMETERS)

After defining the plant that rules the dynamic behavior of a single goniometer, the next step is to design the controller for this degree of freedom – considering the effort as the electrical phase. Using the loop shaping technique – such as what has been applied for Short-Stroke –, the blocks present in Table 5 were defined and embedded.

Table 5: Designed Controllers for Goniometers, in Continuous Time Domain

Controller component	BRG
Proportional gain	11000
Lead-lag zero	64 Hz
Lead-lag pole	800 Hz
1st integrator zero	2 Hz
2nd integrator zero	3 Hz
2nd order low pass filter freq.	1200 Hz
2nd order low pass filter damp	0.13

CLOSED-LOOP RESULTS (GONIOMETERS)

This section presents the results for closed-loop control, considering the goniometers and the designed controller, shown in the last section. Two important events that happen during the operation of a single goniometer will be emphasized in this section: phasing and movement.

Phasing

The phasing procedure is basically applying a ramp in the magnetization current that belongs to the com-mutation architecture – the ramp is present in the FPGA. This avoids rough components in the goniometer and preserves its integrity. By increasing the magnetization current and keeping the general commutation in closed loop, the typical result is shown in Fig. 12. As the magnetization current does not start to feed the goniometer as a step, there are no rough pushes during the phasing.

Figure 12: Position error during phasing.

Movement

With the designed controller and the proposed commutation architecture, it was possible to reach 2.5 °/s for HD-DCM-Lite, a substantial value for the laboratory. Indeed, changes on energy selection by the monochromator can be done in a quick manner, improving the realization of different experiments under different conditions in short periods of time. An example of a movement in terms of feedback and following error at this velocity is shown in Fig. 13.

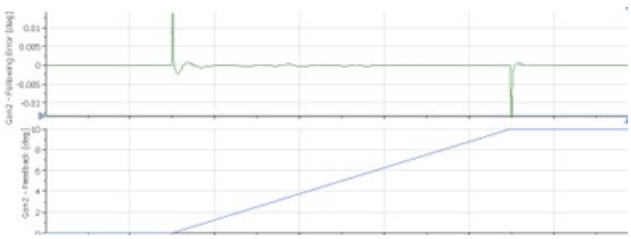

Figure 13: Movement from 0 to 10 degrees

FPGA OPTIMIZATIONS

With the intention to build a set of mechatronic tools to be propagated to other subsequent systems at Sirius, the operating code of HD-DCM-Lite is being developed and validated with several implementations that involve high-performance calculations, timing optimization and serialized operations. Thus, the maximized developed tools allow high performance and resource optimized implementations, attending the majority demanding of high dynamics control systems [16, 17] at Sirius. Some examples are described below.

Homogeneous Transformations Serializations

These operations, essential for kinematic conversions in the Short-Stroke control (represented by T_u and T_y), for

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the HD-DCM-Lite, are calculated in single precision – increasing the quality of the numerical propagation through the architecture –, and the common blocks for single precision calculation in LabVIEW FPGA demand several resources and the allocation during the compilation might not be the best approach. Besides, the timing – and the determinism – is not guaranteed. So, a homogeneous transformations calculator has been developed and it runs inside a single cycle timed loop (SCTL) [18] in FPGA (attached to a derived clock of 20 MHz). The calculation is serialized in such a way that the final values of the transformation come after 3 ticks of 20 MHz (one for each degree of freedom) – and the determinism is guaranteed by the SCTL compilation. Also, the multiplications and sums implement the Xilinx IP library [19], that has high performance packages, to accomplish with the 20 MHz clock [20]. The loop responsible by the control architecture (homogeneous transformations and controller) is a common while loop – as it runs in 20 kHz – and the data is transferred from and to the calculator through memory blocks, guaranteeing a fast data stream from one region of FPGA to the other one.

Transfer Functions Solver

Transfer functions, that represent the controllers that run in the FPGA, depend on past values managed with block memories – differently from the homogeneous transformations, that depend only on actual values – and involve several single precision calculations, depending on the order of the discretized functions. For an example: a low-pass filter is a 2nd order transfer function, while the integrator is a 1st order. To accomplish the required timing, the transfer functions calculator was implemented in a single cycle timed loop with a 50 MHz.

The mentioned implementations optimized the FPGA resources substantially, since homogeneous transformations instead of allocating 6 arithmetic group, a serialized loop runs an arithmetic group 6 times.

SCAN PERSPECTIVES

The implementation of two parallel goniometers – despite the individual controller, in this moment of the offline commissioning – has opened new perspectives on scan, which is an operating mode that is essential for QUATI beamline. The effort applied by the two goniometers has allowed the monochromator to reach high amplitudes in low frequencies (for example: 5° at 1 Hz) and low amplitudes in high frequencies (for example: 0.01° in 20 Hz). An example of the first case is shown in Fig. 14.

To accomplish with the acceleration and deacceleration moments of the scan, a feedforward controller was necessary. It is actually applying a simplified calculation that receives the desired acceleration and multiplies by gains at an order of greatness of 10^6. This feedforward controller is preliminary and will be improved in the next few months during the online commissioning.

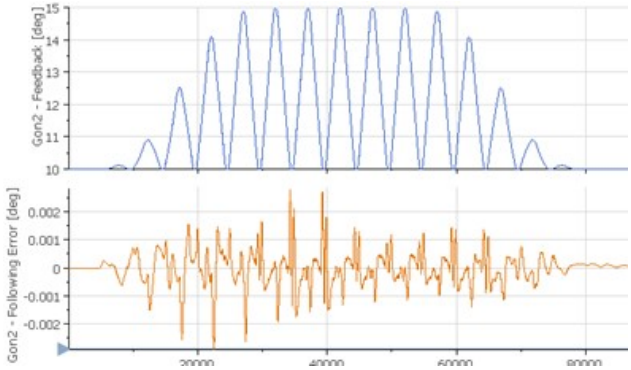

Figure 14: Example of scan at 1 Hz and 5°, done with two goniometers.

CONCLUSION

By looking at the offline commissioning results, the main conclusion is that the HD-DCM-Lite is going through to a delivery that will accomplish with the requirements by QUATI and SAPUCAIA beamlines.

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